



Phase 1 Online SW Status

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- Activity
- Plans



FTM (Juraj)

SW status

- ♦ Progressing with python version of interfaces
 - Writing in parallel with FW progress
 - Current stable version in fexComponents/python
<https://svnweb.cern.ch/trac/atlastdaq/browser/LVL1/l1calo/fexComponents/trunk/python>
- ♦ First version of C++ classes for FTM, in package ftmControl
 - Very similar to structure of efexControl package
- ♦ Partition for FTM tests defined (BhamFexTest, thanks to Rhys)
 - Problems to run (rm_server missing, can't start pmg servers)
 - ???
- ♦ New testrig in PB8 in progress, new rack/servers mounted, being installed now
- ♦ (almost) converged on address map for FTM



eFEX (Rhys)

eFex Software Status

- Currently have a “full” skeleton of classes (1 Control + 4 Processor)
 - ▶ Not much more progress on this front since last meeting
- Implementing improvements based on feed back to interface class generator.
- Working with Juraj to fill common code or code which we think could be common in “fexComponents” package
- Plan to include python quick scripts and TDAQ compatible C++ versions.

More details on the code generator idea:

Instead of code with IPbus nodes as strings like:

```
myDevice.getNode("myRegister").write(someValue);
```

generate class from the IPbus address file and do:

```
myGeneratedDevice.myRegister.write(someValue);
```

Typos in register names picked up at compile time,
not left to run time.



jFEX

- Skeleton “moduleControl” class cloned from eFEX example

- So far by Rouven Spreckels
- New student (Holger Herr) will join the SW effort



- Lots of work on code for Zynq processor
 - Zynq exposes firmware registers to web
 - Giordan's "ironman/jarvis" development:
 - Interface firmware registers in Zynq via on board software to present an IPbus API to external software
 - Exchanges started between gFEX team and Dave Sankey (and myself) on some of the details
 - Whether all gFEX FPGAs would be accessed via Zynq or separately?
 - Long term support of on board OS?
 - Meanwhile we just discovered that in CMS the Wisconsin group has developed something similar
 - Not sure what to do about this
 - Single SW development for Zynq might save global LHC effort, maybe better long term maintenance, but also comforting to have SW under our control



HUB, ROD and FOX

- ROD

- To be started soon...
 - DaveS and I will visit Cambridge at some point

- HUB

- We also need to start with this soon
 - Interaction between HUB and ROD developments?

- FOX!

- No software to configure it of course, but we might like a software/database description of the connectivity?



Next Steps

- Meetings, meetings

- We had one meeting to kick off discussions of what we are all doing, or should be doing, or plan/hope to be doing
- We should continue this on some cycle - eg every couple of months to start with perhaps? More often than joint meetings anyway

- Working sessions

- Gathering experts for SW development weeks was useful in the past, often links to HW development weeks in test rigs
- Again, where, when, how often, etc?