Online Software Status

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- Status and Recent Progress
  - Concentrating on hardware configuration SW
    - Separate talks on simulation and monitoring
- To Do Lists and Timescales

TDAQ, Offline, etc

- New TDAQ release imminent
  - tdaq-05-05-00 being tested in current technical run
  - As from today it is now the default version at point 1
    - Fortunately we (just) already have an L1Calo release for it
  - No API changes - but now includes uhal (IPbus) 2_3_3
    - At least uhal without the controlhub (being discussed with Reiner Hauser)
- Latest Athena release 20.1.0
  - Expecting later versions...?
- Trigger menu
  - Now the CTP is upgraded we can use real Run 2 menus
    - Run 2 supermaster key 2000 - available but not yet tested in L1Calo

Preprocessor

- Recent progress
  - Online SW updated to support new nMCM firmware features
    - SatBCID, 2nd LUT, pedestal corrections (both HW and simulation)
    - Bytestream decoders updated to support new readout modes
      - Decoder for compressed mode still to be tested (waiting for the firmware!)
- To do list
  - M8: support for next FW version (autocorrelation: trivial?)
  - Pedestal correction
    - VME monitoring: FW probably post M8, basic SW support when needed
    - Control SW: when FW is available
  - PHOS4 run and pulser timing: after 16 Feb (before splashes?)
  - Database: changes being finalised: SW work starting ~now
  - Rate metering SW update (2nd LUT, also CMX)
  - Various cleanups and configuration improvements...
  - nMCM serial number to IGUI

CPM and JEM

- Recent progress
  - Reset registers in JEM to recover 160 MHz clock
    - Still some problem with the Jet FPGA?
- To do list
  - ?

CMX (1)

- Recent progress
  - cmxServices fairly complete and stable
    - Geographical address, FW reload & check FW versions, backplane masks from DB (not cables yet?)
    - Configure spy memories, deskew1&2 clocks, reset clock mgr, check PLLs
    - Set readout parameters: NB special mystery setting for cp0
    - Load menu thresholds, reset clocks (again?) and counters
    - Publish some status information to IGUI
  - Standalone programs
    - Write compact flash via VME
    - Determine deskew1&2 phases, monitor miniPODs, stress test logic, diagnose CMX via spy memories ("even user friendly")

CMX (2)

- To do list
  - Set fine delays from DB [soon]
  - Set detailed internal readout latencies [needs DB work]
  - Set BCID offset [needs DB work]
  - Adapt to new firmware features [when available]
  - Need to understand order of clock resets
  - Write deskew1&2 to DB by calib program [exists, untested]
  - More stress tests…

L1Topo

- Recent progress
  - Keeping up with register model changes
  - Extra test vectors
- To do list
  - Further address file changes (eg for menu loading)
  - Publish more status to the Information Service (IS)
    - And display it: IGUI/web/etc?
  - And surely lots more testing, eg of robust configuration from scratch, resets, incoming and outgoing links, etc?
    - Ensure we have a good order of clock resets between CMX and L1Topo
      - And whats the situation with the MuCTPI interface to L1Topo?
  - Do we want publication of algorithm rates in L1Calo or are rates at the CTP enough?

Database

- COOL Database: not much recent progress
  - Getting urgent to move back to Oracle
  - But new PPM schema still not finalised
  - Also need to finalise less significant changes to other folders
    - Some previously foreseen folders may not in fact be needed
      - Eg optical link settings for L1Topo
  - Need extra readout configuration folders
    - Additional CMX internal latencies
    - Separate latency for L1Topo readout
- Trigger menu
  - Implemented run 2 menu (mostly)
    - L1Calo menu interface had mostly dummy run 2 methods up to now
  - Still to be tested

Miscellaneous

- Trigger monitor
  - New LAr student (Ryne Carbone) has added IS publication of lists of hot LAr towers (as well as existing ERS messages)
- Rate metering
  - Need to add PPM jet LUT and CMX rates (archiving, display)
- Web displays
  - Some old displays still not working
    - Need webis update from Reiner Hauser

Phase 0 (Run 2) Summary

- Lots to implement and test in the next month

Phase 1 Notes: IPbus

- Software discussion yesterday
  - To be summarised by Bruce later
- A few subsequent thoughts on IPbus
  - IPbus based on address files describing the register model
    - Required by software, also used by firmware to generate some VHDL
  - So far (L1Topo) address files stored in software SVN (no git!)
    - Package topoControl, directory ipbus/address
      - Updated there by firmware developer (Christian)
      - Same authorisation (atlas-svn-l1calo egroup) for SW & FW repositories
  - Will be useful to have this (or something) for phase 1 ~now
    - Can create empty(ish) "module services" packages for new modules
      - ftmControl, efexControl, etc
    - Add initial empty(ish) address files, keep them updated there
      - Naming convention from OKS database module types: L1CaloEfex etc
        - Address files for subcomponents at least include which FEX (not "processor.xml"!)
    - Is this OK for firmware developers?