gFEX Connectivity

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- Notes and Caveats
- Numerology
- Conclusions

- (And various backup slides used as input)

Notes

- Check all the sources of fibres to the FEXes
  - LAr DPS in all regions, Tile via JEM and Tile in phase 2
- Look both at baseline 6.4 Gb/s and ~10 Gb/s options
  - NB fewer jFEX fibres at high speed
  - (But assume same number of eFEX fibres - no BCMUX)
- Assume phi ring jFEX in both cases
  - Though this option is not carefully checked at 6.4 Gb/s
  - Phi ring jFEX needs less fanout at high eta
    - But not yet checked in detail
- CAVEAT
  - Plenty of room for mistakes!
    - I have not completely updated my spreadsheets with all the changes consequent on choosing the phi ring jFEX (especially at 6.4 Gb/s)

Summary Table: 6.4 Gb/s

Calo Region	Fibres to eFEX	Fibres to jFEX	Fibres to gFEX	Spare fibres	Coverage (eta*phi)	Supercells & Towers	Need splitter?
EM<2.4	36	8	1	3	0.8*0.4	320 & 32	No
EM>2.4 (separate) Option	20	8	4?	16?	0.8*1.6	160 & 32	No
HEC (separate)	12+14*2	18*2+6	8?	0	1.7*1.6	192	Yes: 1->3 if gFEX?
HEC+ EM>2.4 Option	10*2 +10	12*2 +4	6?	2?	1.7*0.8 0.8*0.8	80 & 112	Yes
FCAL	0	24	4?	20?	1.7*1.6	192	No
Tile/JEM (BCMUX)	12?	8?	2	?	0.8*0.4 0.8*0.6	32 48	Yes?
Tile/ROD	20	16	2	?	Assume 1.6*0.4	64	No

Summary Table: 10 Gb/s

	Calo Region	Fibres to eFEX	Fibres to jFEX	Fibres to gFEX	Spare fibres	Coverage (eta*phi)	Supercells & Towers	Need splitter?
	EM<2.4	36	6	1	5	0.8*0.4	320 & 32	No
Option	EM>2.4 (separate)	20	8?	4?	16?	0.8*1.6	160 & 32	No
Option	HEC (separate)	18	12+10*2	8?	~0	1.7*1.6	192	Yes if gFEX
Option	HEC+ EM>2.4	12 +10	15 +4	6?	~1	1.7*0.8 0.8*0.8	80 & 112	NO!
	FCAL	0	16	4?	28?	1.7*1.6	192	No
	Tile/JEM (BCMUX)	6	6	2?	?	0.8*0.4 0.8*0.6	32 48	Maybe if gFEX?
	Tile/ROD	12	12	2	?	Assume 1.6*0.4	64	No

Conclusion

- Can provide gFEX outputs from LAr DPS & Tile JEM
  - Most congested for HEC
    - Prefer DPS FPGAs combining HEC and EM>2.4
- Adding gFEX increases complexity
  - Adds/requires extra optical splitting in some places
    - Possibly need 1->3 splitting from HEC at 6.4 Gb/s?
      - Forces eFEX and jFEX outputs to have same geometry => implication for FEX layout?
  - All DPS/Tile output fibre bundles have a fibre to gFEX
    - Even less likely to be able to use off the shelf fibre rebundling
- But no showstoppers....?

Backup

gFEX Inputs Requirements(?)

- One fibre per 0.8*0.4 in eta*phi (per layer)
  - Corresponds to one LAr DPS FPGA (|eta|<2.4)
  - Eight 0.2*0.2 jet elements
- Roughly 16*8*2=256 fibres for |eta|<3.2 (EM+Had)
  - Few extra for FCAL
  - No on board fanout => 60-80 inputs per FPGA
- Independent of link speed
  - At high speed just add more data (resolution & coordinates)

LAr DPS Outputs to gFEX (1)

- EM Barrel and standard EM Endcap (|eta|<2.4)
  - One DPS FPGA covers 0.8*0.4 = 32 towers, 320 supercells
  - 48 output fibres: single 48 fibre bundle
  - Up to 36 fibres to eFEX, 8 to jFEX: >1 spare for gFEX
    - Down to 6 jFEX fibres at 10 Gb/s (with larger jFEX environment)

- Forward EM Endcap (2.4<|eta|<3.2)
  - One DPS FPGA covers quadrant: 32 towers, 160 supercells
  - Original calculations assumed eta slice jFEX
  - Up to 20 fibres to eFEX, 16 to jFEX: >1 spare for gFEX
  - With phi ring jFEX this region needs no fanout? (Check!)
    - If so, only need 8 fibres to jFEX (at most): masses of spares
    - Further reduction in jFEX fibres at 10 Gb/s

LAr DPS Outputs to gFEX (2)

- HEC
  - One DPS FPGA covers quadrant (1.6 in phi): 192 towers
  - Original calculations assumed eta slice jFEX
  - Up to 20 fibres to eFEX, 24 to jFEX
    - NB almost all those fibres need additional 1:2 splitting
  - But still have a few spare fibres for gFEX
    - But not enough?
    - Unless eFEX/jFEX fibres have more than 1:2 subsequent splitting?
  - With phi ring jFEX the >2.4 region needs no fanout? (Check!)
    - If so, need fewer fibres to jFEX - but not enough to avoid any splitting

LAr DPS Outputs to gFEX (3)

- Combined DPS for HEC+EM>2.4
  - FPGA covers octant (0.8 in phi) all HEC and EM>2.4 region
  - Better use of spare fibres cf separate DPS for EM>2.4
  - At 10 Gb/s can just avoid any further splitting
    - And still room for a few fibres to gFEX
    - My preferred option
  - Could further reduce fibres by summing EM+Had for eta>2.4

- NB there is an alternative proposal (Stefan Simion) to combine EM>2.4 with the standard EMEC region (1.6-2.4) FPGAs

LAr DPS Outputs to gFEX (4)

- FCAL
  - Each FPGA covers half of phi (one side)
  - Originally imagined 48 fibres per FPGA
    - Fanout to two adjacent jFEX modules in eta slice jFEX scheme
    - 8 cells/fibre (as for jFEX towers) allowing ~15 bits/cell
  - No spares!
  - Options:
    - (a) With 10 bits/cell, jFEX fibre count reduces to 32
    - (b) With phi ring jFEX no need to fan out FCAL cells => 24 fibres
  - Summary: can have spare outputs for gFEX fibres

Tile Outputs to gFEX

- Phase 1: via JEM
  - One FPGA covers either 0.8*0.4 or 0.8*0.6 in eta*phi
    - Irregular geometry
  - Inputs are BCMUXed: assume same for outputs
    - Saves factor two in number of fibres
  - Probably one minipod per FPGA - but might squeeze on two?
    - Either 12 or 24 output fibres per FPGA
  - Up to ~9 fibres to eFEX, ~8 to jFEX (varies per FPGA)
    - Four different contents with masses of fanout due to ugly geometry
  - Expect 1 or 2 gFEX fibres (varies per FPGA)
  - OK with optical splitting (if only one minipod per FPGA)

- Phase 2: from new Tile electronics
  - Presumably design it with gFEX in mind if needed