gFEX Functionality via jFEX?

Murrough Landon
(On behalf of gFEX
hardware review panel)
5 December 2013

- Introduction
- Phi ring jFEX
- Pileup calculations
- Fatter jets (in phi and eta)
- Summary

gFEX Hardware Review Panel (1)

- Composition:
  - Ian Brawn, Weiming Qian, Murrough Landon, Sam Silverstein, Uli Schaefer, Eduard Simioni, Stefan Rave, Esteban Fullana Torregrosa
- Three meetings so far:
  - https://indico.cern.ch/conferenceDisplay.py?confId=283506
  - https://indico.cern.ch/conferenceDisplay.py?confId=283766
  - https://indico.cern.ch/conferenceDisplay.py?confId=285494
- Useful email interactions with physics experts
  - David Strom, Michael Begel, Alan Watson, Jim Linneman

gFEX Hardware Review Panel (2)

- Scope
  - Can the gFEX functionality can be implemented in the current baseline system ?
- Fat jets
  - Target: 2.0 x 2.0 (1.8 x 1.8 = gFEX TDR)
  - jFEX & jFEX–Topo solutions
- Pile up
  - ρ parameter
  - ϕ rings, 0.2 in η
  - jFEX & jFEX–Topo solutions
- Requirements for the above
  - Bandwidth: in/out modules, between FPGAs
  - Link Speed
  - Mapping
  - Constraints placed on algorithms

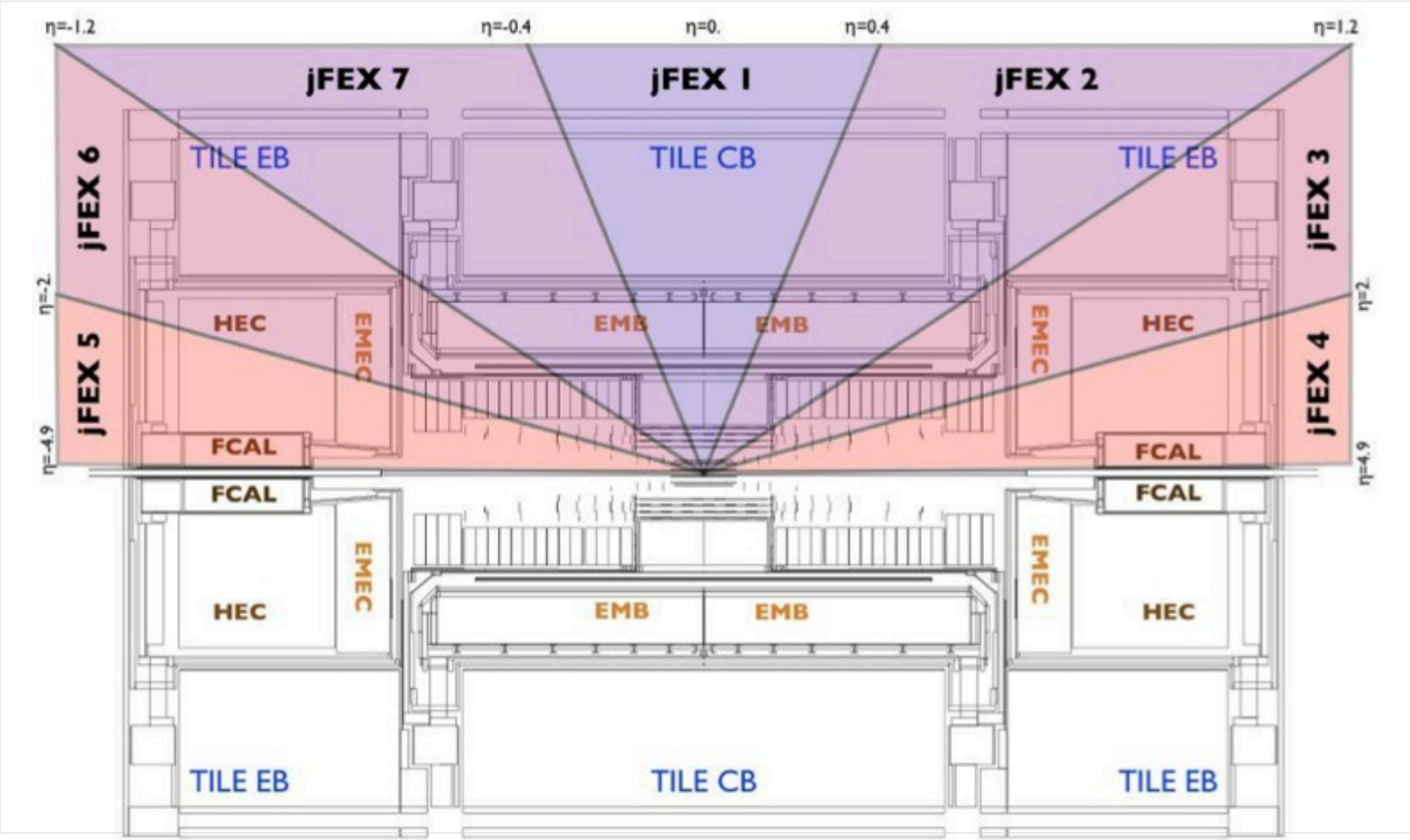
Approach

- Play devils advocate and try to avoid gFEX hardware
  - Can requested gFEX functionality be provided by jFEX?
- Physics panel investigating baseline jFEX+L1Topo
  - With 6.4 Gbit/s links the maximum jFEX jet size is 0.9*0.9
  - Fat jets only possible by composition of 0.9*0.9 in L1Topo
  - Pileup subtraction at L1Topo using mean of Et medians in several eta strip oriented jFEX modules
- Hardware panel has looked at extending the baseline
  - Suggest phi oriented jFEX with ~10 Gbit/s links
  - Maximise jet size
  - Use data sharing between FPGAs for local pileup subtraction

Phi Ring jFEX

- TDR jFEX assumed to cover eta strips (0.8 in phi)
  - Same geometry originally assumed for higher speed option
- Now looking at jFEX modules oriented as phi rings
  - Input links at ~10 Gbit/s (~200 fibres/module)
  - Seven jFEX modules in the system (cf eight for eta strips)
    - Module core area: 0.8 in eta * all phi (larger eta at the ends)
  - Four big FPGAs per module
    - FPGA core area 0.8*1.6 in eta*phi
  - Environment +/- 0.8 at 0.1 granularity
  - Schemes for additional "frame" of 0.2*0.2 jet elements
  - Maximum jet size 2.2*2.2 in eta*phi sliding by 0.2
  - Pileup subtraction on jFEX module
    - Needs exchange of data between FPGAs

Phi Ring jFEX Layout



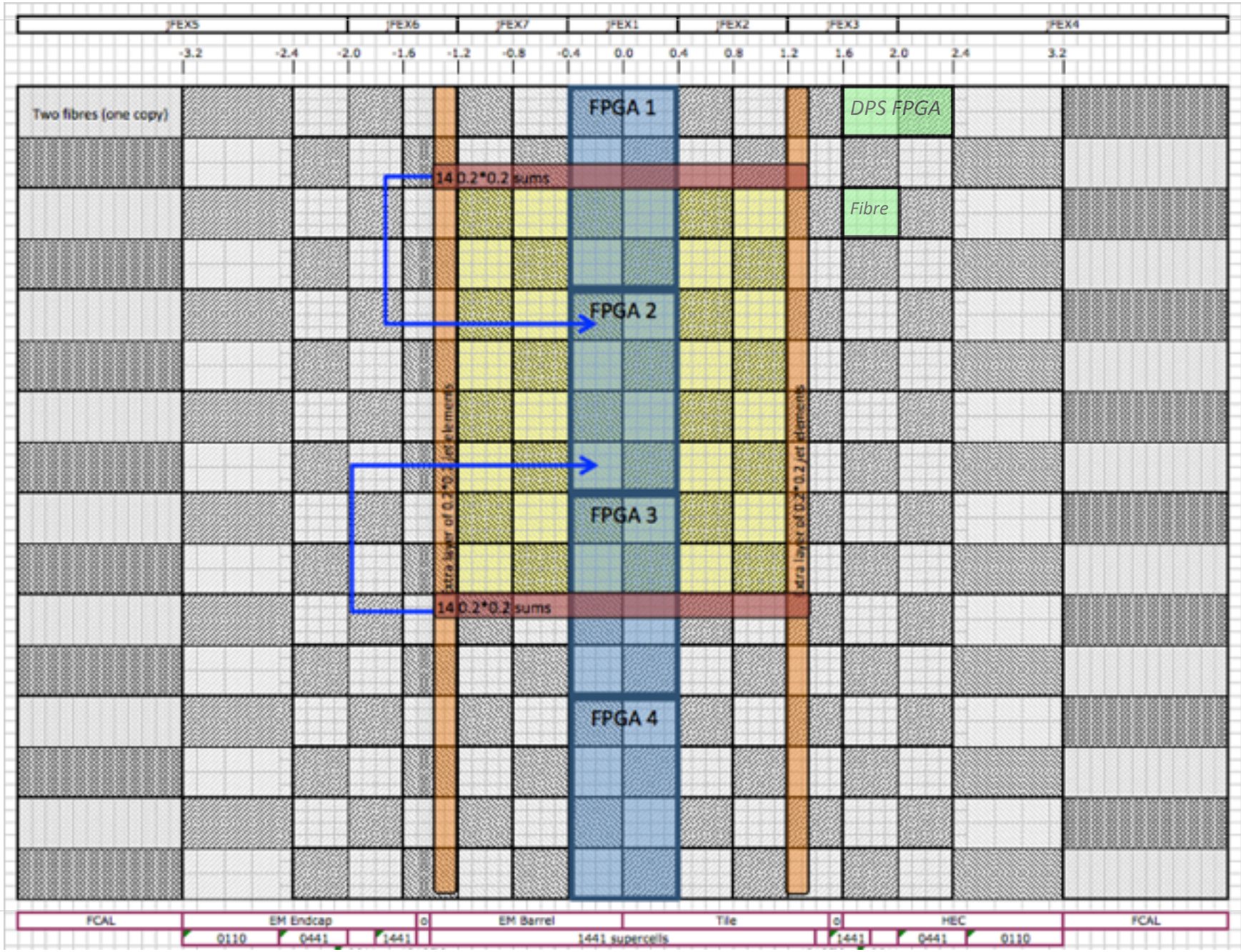
Calculating Pileup: Phi Ring jFEX

- Ideal case (gFEX): whole phi ring in one FPGA
  - But even phi ring jFEX module still splits phi into 4 FPGAs
- Share pileup estimates between jFEX FPGAs
  - Bandwidth available on low latency 1 Gbit/s links (25 bits/BC)
  - Maximum 240 links/FPGA of which ~140 already required for configuration/control (via IPbus), merging results to L1Topo, handling HEC overlap, extended environment in eta (see later)
- Use 42 links per FPGA (7 links * 2 ways * 3 FPGAs)
- Can send one 12 bit pileup estimator per 0.2 in eta
  - Either median Et, thresholded SumEt or (DavidS) histogram?
    - If possible just use the core 1.6 in phi per FPGA
      - Using full 3.2 phi environment available in each FPGA costs 1 BC latency penalty
  - Combine estimators (mean?) from each FPGA to derive rho
  - Subtract pileup from jets and missing Et components
    - Send pileup subtracted jets and missing Et to L1Topo

Fat Jets: Introduction

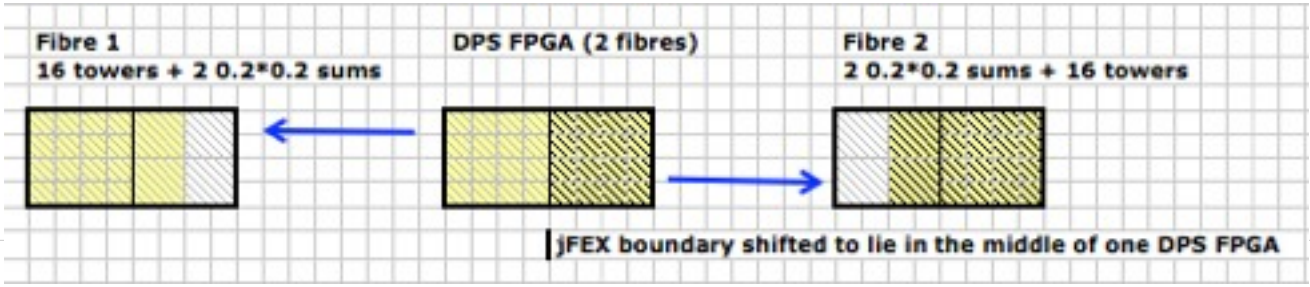
- 10 Gbit/s jFEX offers 1.7*1.7 jets sliding by 0.1
  - There is 0.8 eta and phi environment around each core tower
- NB jFEX with 0.2 sliding windows offers 1.8*1.8 jets
  - 2*0.8 environment around each tower + core 0.2
  - And gaussian weighting calculations can still be done at 0.1
  - [Reminder: only if we are allowed to assume 10 Gbit/s links]
- Is there any chance of even fatter jets?
  - Consider schemes for fatter jets in phi or eta
  - Only sliding by 0.2 (surely no bandwidth for 0.1)
  - Adding 0.2 each side in both eta and phi gives 2.2*2.2 jets
  - Different solutions needed for eta and phi:
    - eta: squeeze more data onto fibres and reorganise mapping
    - phi: share 0.2*0.2 sums via additional low latency links between FPGAs

Phi Ring jFEX Diagram



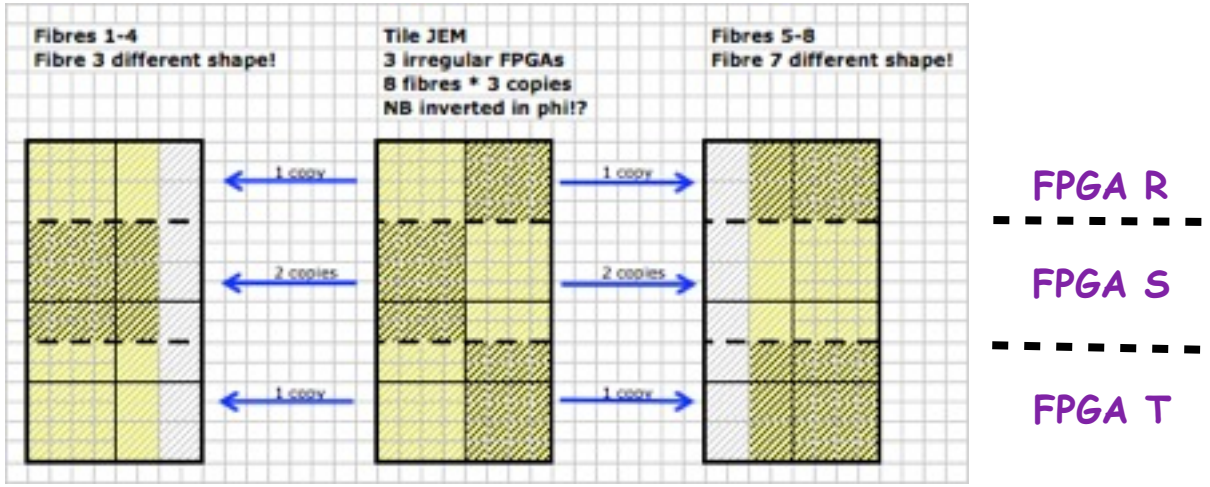
Fatter Jets in Eta

- LAr DPS FPGAs cover 0.8*0.4 in eta*phi (central EM)
  - Original idea for 10 Gbit/s: two fibres covering 0.8*0.2
  - 16 tower/fibre: 11(13) bits/tower at 9.6(11.2) Gbit/s
    - Eg 11 bits allows 0-255 GeV in 128 MeV steps or 0-511 GeV in 250 MeV steps
- Suggestion for fatter jets:
  - Fibres cover 0.4*0.4 in eta*phi
    - Shift core jFEX coverage by 0.4 to span centre of DPS FPGAs
  - Squeeze n.bits/tower and add two 0.2*0.2 sums from the other half of each FPGA (ideally at 11.2 Gbit/s)
    - 16 * 12 bits/tower + 2 * 12 bits/sum = 216 bits + 8 bit CRC = 224 bits
      - Sacrifice any ideas of special Ex/Ey/E sums per FPGA on these fibres?
  - Can have 2.2*1.8 (eta*phi) jets sliding by 0.2



Phi Ring jFEX: Tile Inputs

- Phase 1
  - Division of JEM towers into FPGAs is awkward!
  - Ugly solution is possible with some 0.4*0.6 shape fibres
    - At phase 1 we have 8 bits/tower BCMUXed => 9 bits for 2 towers
    - Can easily fit 24 towers per 9.6 or 11.2 Gbit/s fibre
      - The neighbouring 0.2*0.2 areas would also be 6 pairs of BCMUXed towers in this case
        - 12*9 bits + 6*9 bits = 162 + 8 bit CRC = 170 bits



- Phase 2
  - Require TileCal to commit to 0.4*0.4 fibres ~now!
    - There may be a latency impact for necessary regrouping…

Phi Ring jFEX: HEC Overlap

- In phi ring, HEC overlap towers are all in two modules
  - And required in neighbouring modules as environment
  - (Unlike original eta strip jFEX where all modules suffered a small amount of barrel/endcap transition)
- Three approaches for handling this
  - (1) Drastic: drop HEC overlap (1.5<|eta|<1.6) for periphery
    - Only jFEX modules where overlap region is in the core get them
    - Efficiency loss - but in a region where efficiency suffers anyway
  - (2) Squeeze overlap towers onto same fibres as 1.6<|eta|<2.0
    - Resolution down to 10 bits/tower and 8 bits for 0.2*0.2 sums
      - 20*10 bits + 2*8 bits = 216 bits + 8 bit CRC = 224 bits at 11.2 Gbit/s
      - Not really an option at 9.6 Gbit/s
  - (3) Send HEC overlap on separate fibres
    - Need to receive them in separate FPGA and transfer over low speed links
    - Extra minipod and PCB tracks used on just two jFEX modules

Fatter Jets in Phi

- Share rows of 14 0.2*0.2 sums to neighbour FPGAs
  - Sums made from core towers so no latency impact
    - 1 BC in the shadow of the PMA loopback of environment towers
- Per FPGA need two rows sent and received
  - Two sums per link (25 bits/BC per 1 Gbit/s link)
  - Total of 28 links if EM+hadronic already summed
    - Would need 56 links for EM and hadronic separately: too many?
  - Certainly 28 links seems viable
  - Can have 1.8*2.2 (eta*phi) jets sliding by 0.2
- Can use both fatter eta and phi schemes
  - Maximum jet size up to 2.2*2.2 sliding by 0.2
    - Core 1.8*1.8 has 0.1*0.1 granularity (gaussian weighting calculations?)
  - Can still make smaller jets (up to 1.7*1.7) sliding by 0.1

Summary

- Provisional hardware panel conclusion
  - gFEX functionality could be done in 11.2 Gbit/s phi ring jFEX
    - Which could provide even fatter jets (2.2*2.2) than TDR gFEX
  - 9.6 Gbit/s links are probably enough - but not comfortable
    - And HEC overlap towers would need to be on separate fibres
- But nothing comes for free!
  - Price includes one or more of: fewer bits/tower, loss of efficiency/resolution for HEC overlap, extra complexity of jFEX PCB, 0.4 phi modularity in Tile at phase 2
- Some questions still to be resolved
  - Eg, are suggested pileup subtraction algorithms sufficient?
  - Check bandwidth to L1Topo: fat+thin jets, Et, fat taus, etc?
- Uncertain link speed means we cannot choose now

Postscript: 6.4 Gbit/s jFEX

- Hardware panel did not discuss 6.4 Gbit/s options
  - Assumed maximum 0.9*0.9 jets too far from target 2.0*2.0
- My **personal, last minute, unreviewed** thoughts....
  - Apply fatter eta and phi schemes to baseline 6.4 Gbit/s jFEX
  - Phi ring jFEX at 6.4: FPGA environment 1.6*2.4 in eta*phi
    - Provides 0.4 environment each side of 0.1*0.1 tower => 0.9*0.9 jets
  - Fibres: eight 0.1*0.1 towers (0.4*0.2) + two 0.2*0.2 sums
    - Maximum jet size extended to 1.8 in eta (sliding by 0.2)

  - Add extra 20 links for phi sharing (48 links total)
    - Share two rows of 0.2*0.2 jet elements in phi at 12 bits/sum
    - Or three rows by squeezing to 8 bits/sum (quad linear encoding)
  - Maximum jet size possibly 1.8*2.2 in eta*phi
    - Michael Begel already gave his opinion of non-square jet windows:
      - Very ugly, horrible acceptance problems, only do this if we are absolutely desperate
  - But maybe as fallback if 10 Gbit/s option doesnt work???

Backup

L1Topo Inputs: Phi Ring jFEX

- Proposal for 7 phi ring jFEX modules
- L1Topo FPGA1:
  - 48 eFEX EM fibres (2/eFEX module)
  - 28 jFEX jet fibres (4/jFEX module)
  - 4 muon fibres (NB copied to both FPGAs)
  - No spare fibres
- L1Topo FPGA2:
  - 48 eFEX Tau fibres (2/eFEX module)
  - 7 jFEX energy sum fibres (1/jFEX module)
    - Assuming a small number of Ex/Ey and Et sums (eta granularity?)
  - 4 muon fibres (NB copied to both FPGAs)
  - 21 spare fibres (presumably some for fat taus?)
- Could accept more energy fibres/jFEX

Calculating Pileup: Eta Strips

- Eta strip jFEX must send pileup estimates to L1Topo
  - Jets and Et sums are sent before pileup subtraction
- jFEX at 10 Gbit/s: 0.8 phi core + 2 * 0.8 environment
  - So each jFEX sees 24 of the total 64 phi bins
  - Eta range is 82 bins (50 central, 8 forward, 2*12 FCAL1)
  - Assume 11.2 Gbit/s fibres => 216 data bits per fibre
  - Say 8 bits per pileup estimate => 27 possible values
    - Roughly one pileup estimate per 3 eta bins
- Et components need more bits (~24)
  - Et magnitude and direction above and below threshold
  - Another two fibres per jFEX
  - Viable but L1Topo getting rather full of jFEX fibres
- Total ~ 6 fibres per jFEX to L1Topo (48 total)

L1Topo Inputs: Eta Strip jFEX

- Proposal with 8 eta strip jFEX modules
- L1Topo FPGA1:
  - 48 eFEX EM fibres (2/eFEX module)
  - 24 jFEX jet fibres (3/jFEX module)
  - 4 muon fibres (NB copied to both FPGAs)
  - 4 spare fibres
- L1Topo FPGA2:
  - 48 eFEX Tau fibres (2/eFEX module)
  - 24 jFEX energy sum + pileup estimate fibres (3/jFEX module)
    - Assuming a small number of Ex/Ey and Et sums (eta granularity?)
  - 4 muon fibres (NB copied to both FPGAs)
  - 4 spare fibres
- Not much left (fat taus?)

Low Latency Link Count

- Low latency 1 Gbit/s links are used for many things
  - Control and configuration (via IPbus): 25?
  - Result merging to L1Topo: 72
  - HEC overlap (inputs fibres to separate FPGA): 17
  - Pileup data sharing: 42
  - Fatter phi: 28
  - Total so far: ~180
  - Maximum available per FPGA: 240