L1Calo: FEX Inputs

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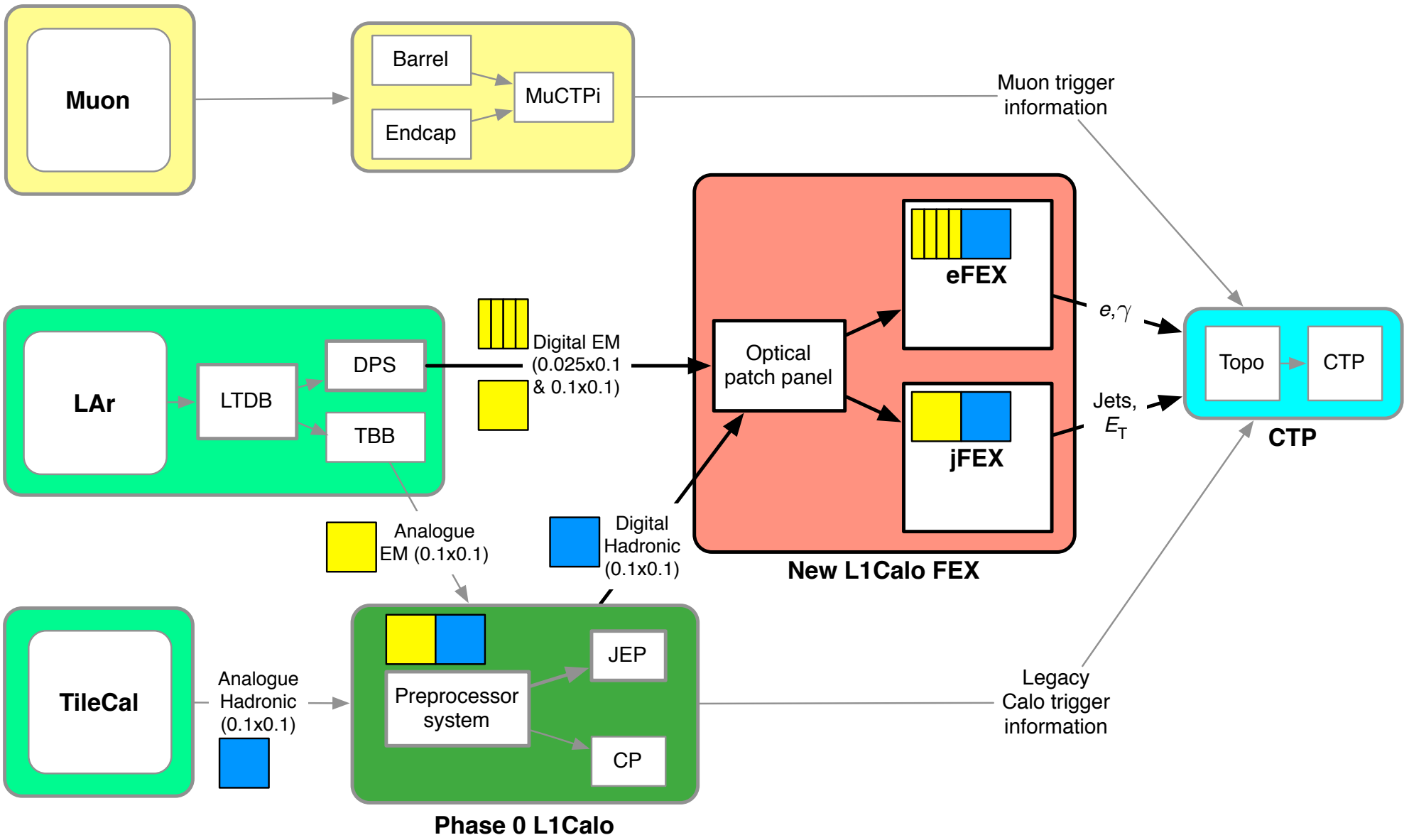
(NB some overlap with BCMUX talk by Steve)

- Overview
- Link technical details: speeds, encoding, etc
- eFEX inputs: EM & Hadronic layers
- jFEX inputs
- Handling Tile signals (until phase 2)
- Optical patch panels
- Conclusions

Overview


Muon
Barrel
Endcap
MuCTPi
Muon trigger information
LAr
LTDB
DPS
TBB
Digital EM (0.025x0.1 & 0.1x0.1)
Optical patch panel
eFEX
jFEX
e,γ
Jets, E_T
Topo
CTP
CTP
Analogue EM (0.1x0.1)
Digital Hadronic (0.1x0.1)
New L1Calo FEX
TileCal
Analogue Hadronic (0.1x0.1)
Preprocessor system
JEP
CP
Legacy Calo trigger information
Phase 0 L1Calo

Link Technical Details

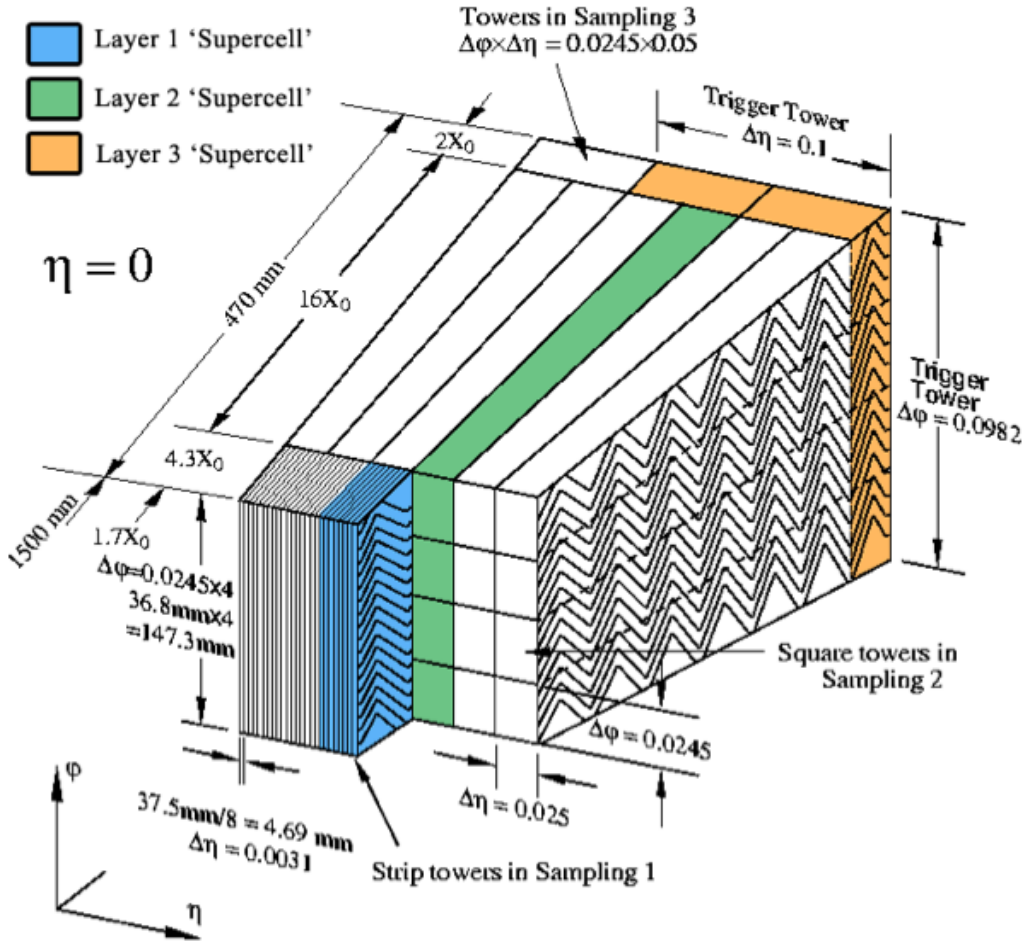
- TDR Baseline
  - Link speed: 6.4 Gbit/s with 8/10 bit encoding
  - Allows 128 data bits per fibre per BC
  - Reserve ~8 bits for checksum: 120 payload bits for trigger
- Higher speed under study
  - Very promising results from recent 10 Gbit/s tests
    - https://indico.cern.ch/getFile.py/access?contribId=12&sessionId=1&resId=1&materialId=slides&confId=250100
  - Can get up to ~200 usable bits per BC
    - Requires custom encoding scheme (eg 64/66 bit) - to be investigated
  - Needs testing in real prototypes before changing baseline

Connectivity and Mapping

- Connectivity and mappings define the architecture
  - To be fixed early: detailed discussions under way with LAr
  - But link contents and speeds may change
- Two granularities to consider
  - Fine granularity supercells for EM layer to eFEX
    - Two 0.1*0.1 towers per link with ten supercells each (20 supercells/link)
    - At 6.4 Gbit/s this requires use of the "BCMUX" compression scheme
  - Traditional 0.1*0.1 towers for jFEX & hadronic layer to eFEX
    - Eight towers per link at 6.4 Gbit/s
    - EM and hadronic towers summed in depth (EM and hadronic separate)
    - Coverage 0.4*0.2 in eta*phi (best match to future Tile phase 2 RODs)
- Options for higher speed links
  - EM supercells: still 20 supercells/link but no need for BCMUX
  - Towers: possible increase to 16 towers per link

Link Contents (1)

- High granularity EM layer supercells
  - 10 supercells per traditional 0.1*0.1 trigger tower
    - 1 Presampler, 4 Front, 4 Middle, 1 Back layer
  - Baseline: Et with ~10 bits dynamic range per supercell
    - Eg 256 MeV to 256 GeV (maybe one extra bit for middle layer)
  - Result ~100 bits per tower
  - With BCMUX ~110 bits per two towers => one link



Link Contents (2)

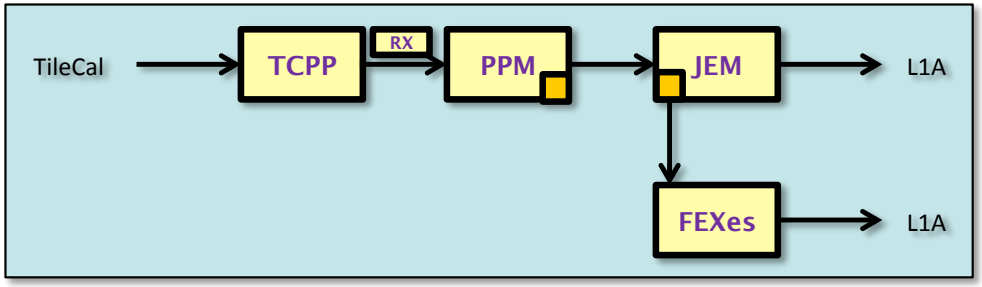
- Traditional 0.1*0.1 towers
  - Baseline: Et with up to ~13 bit dynamic range
    - Possibility to top slice some bits for Energy sums in larger area
- FCAL
  - Supercells at finer granularity than present FCAL towers
    - 12 FCAL1 + 8 FCAL2 + 4 FCAL3 supercells per 0.4 in phi (cf 4+2+2 now)
    - Eight FCAL supercells per link with Et up to ~13 bits per supercell

TileCal Inputs for Phase 1 (1)

- Digital Tile signals are scheduled for phase 2
  - Until then we still have the existing analogue signals
- Need digital inputs to the FEXes for phase 1
  - Three options described at the TDAQ IDR in January
  - (1) New Tile digitiser boards and additional DPS modules
  - (2) New optical outputs on PPM rear transition card
  - (3) New optical outputs on JEM input module (plus PPM mods)
- Options considered in detail by expert panel
  - https://twiki.cern.ch/twiki/bin/viewauth/Atlas/TileInputOptions

TileCal Inputs for Phase 1 (2)

- Recommendation: prefer option 3 as baseline



- Fallback to option 2 (better tested) if 3 has problems
- Reconsider option 1 if use if further simulation (to be done) shows separate digitisation of Tile D cells would be useful

Fanout & Optical Patch Panels

- FEX sliding window algorithms require lots of fanout
  - FEX modules need "environment" around a core processed area
  - Need ~2 identical copies of each link (to adjacent modules)
    - For hadronic layer need 4 copies: 2 for eFEX, 2 for jFEX
  - EM layer: two copies provided at source by the DPS
  - For HEC we will need additional 1:2 passive optical splitting
  - Selected Tile input option should provide all copies at source
- Optical patch panels
  - Fibre ribbons from LAr DPS and Tile will need reorganising to suitable grouping for input to eFEX and jFEX
  - Optical patch panel plant required to do this

Summary

- Baseline defined for FEX input links at 6.4 Gbit/s
  - Speed may increase if tests are successful (we hope!)
    - No impact on eFEX architecture (drop BCMUX, change encoding)
    - Would allow more towers/link to jFEX => larger jet sizes
- Tile inputs baseline chosen as "option 3" (via JEM)
  - TDR section needs updating to reflect this choice
- Further work
  - Define detailed mappings from LAr front end to FEXes
  - More simulation to refine dynamic ranges, encoding etc