Mappings from DPS to FEXes

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- Introduction
- Original and new eFEX/jFEX mappings
- Fanout patterns from DPS FPGA
- Use of higher speed links?
- Guide to spreadsheet (NB its a work in progress)

Reminder: eFEX & jFEX

- eFEX (UK)
  - EM and Tau triggers
    - Recent decision: baseline 0.3*0.3 environment
      - No physics case for larger environments (eg present 0.4*0.4) due to pileup
  - EM layer: new supercells
  - Hadronic layer: plain old 0.1*0.1 towers (HEC and Tile)
  - FCAL: not used
- jFEX (Mainz)
  - Jet and energy triggers (maybe also larger Tau trigger?)
  - EM and hadronic: plain old 0.1*0.1 towers
    - Change from present system which uses 0.2*0.2 jet elements
  - FCAL: new finer granularity to improve XE and Fwd jets
  - Baseline: max jet size 0.9*0.9 (present 0.8*0.8)
    - Good physics case to try to increase this if possible

DPS-FEX Fibre Basics

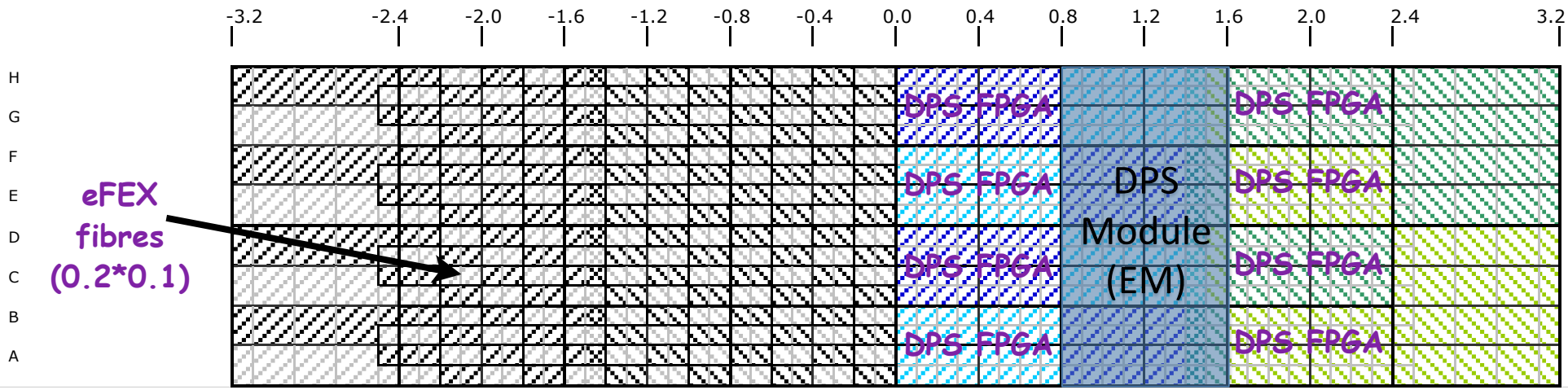
- EM layer: two different granularities
  - Fine granularity supercells to eFEX, towers to jFEX
  - eFEX fibre: 20 supercells (two adjacent 0.1*0.1 towers)
    - Currently proposing adjacent in eta as eFEX is longer in eta than phi
    - Need to use the BCMUX scheme at 6.4 Gbit/s
  - jFEX fibre: eight 0.1*0.1 towers (summed supercells)
- Hadronic layer: same granularity to eFEX and jFEX
  - Same as EM jFEX fibre: eight 0.1*0.1 towers
- Baseline link speed 6.4 Gbit/s
  - But see later...

Original Mapping Ideas

- Original eFEX and jFEX designs: strips along eta/phi
  - One module to cover all eta (or phi) and strip of phi (or eta)
  - Not the best shape, but simple fanout request from DPS
    - Two copies of every fibre satisfies fanout requirements everywhere
- However…
  - Challenging eFEX design and extremely challenging jFEX
- So…
  - New baselines have modules covering subset of eta and phi
  - Squarer shapes more efficient, but introduce "corners"
    - Parts of the eta phi space need four copies, some just one (eFEX only)
- Which raises the question…
  - Can the DPS do more complex fanout patterns?
    - Within the currently expected limit of four output ribbons of course!

Coverage of DPS AMC FPGA

- My understanding:
  - One AMC handles equivalent of one LTDB: 320 supercells
  - For regular mapping, EM AMC covers 0.8*0.4 in eta*phi
    - For EMEC inner wheel, either 0.8*0.8 or (probably) 0.8*1.6 - not sure??
  - DPS module: 0.8*1.6 may allow barrel/endcap overlap
    - Otherwise no particular constraints from L1Calo
  - In HEC, I guess one AMC covers one quadrant: 192 towers??
  - For FCAL, I guess one AMC covers half of phi: 192 scells??

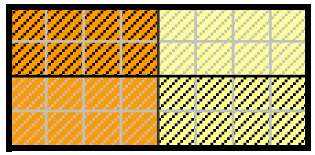


Fanout Patterns from DPS

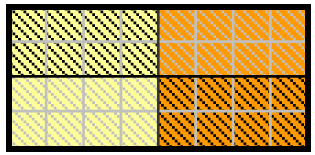
- Can one DPS fanout pattern handle corners?
  - New eFEX baseline no longer needs 2 copies of all fibres
  - But needs four copies in some places
  - New jFEX baseline needs four copies around eta=0
    - jFEX has a possible solution, but fanout at source would be better
- Suggested patterns (see spreadsheet for details)
  - One 36 fibre pattern covers all eFEX cases
    - No DPS FPGA needs to enable all outputs
  - Need two patterns for jFEX (or one reflected at eta=0)

36 fibres

eFEX outputs
1, 2 or 4 copies



12 fibres



12 fibres

jFEX outputs
2 copies everwhere
(except 4 at eta=0)

Higher Link Speeds??

- TDR baseline will be 6.4 Gbit/s
  - But LAr and L1Calo experts plan tests of higher speeds
- Possible uses of higher bandwidth
  - eFEX
    - Considering 9.6 Gbit/s (and 64/66 bit encoding) - but no higher!
    - Same mapping but no need for bandwidth saving "BCMUX" scheme
      - Avoid some inefficiencies at very high luminosity => happier physicists
  - jFEX
    - Strong interest in larger jets (closer to 2*2 than proposed 0.9*0.9)
      - Nice to have 0.1*0.1 sliding windows but already using biggest available FPGAs
    - Higher speeds could be used to supply the environment for larger jets
    - Ideal case: 16 towers per fibre may allow 1.7*1.7 jets
      - Uli (Mainz) is investigating even higher speeds than 9.6 Gbit/s... even more challenging!
  - Questions for LAr DPS
    - What if DPS eFEX outputs use 9.6 but jFEX wants to run higher?
      - EM ribbons: 3 eFEX + 1 jFEX, HEC ribbons: 2 eFEX + 2 jFEX, FCAL ribbons: 4 jFEX

Guide to Spreadsheet

- List of worksheets
  - 1: Summary: a few assumptions
  - 2: Diagram of LTDB layout in the EM layer
  - 3: EM layer DPS: eta-phi coverage of FPGAs & fibres to eFEX
  - 4: Ditto for fibres to jFEX
  - 5: HEC DPS: eta phi coverage of fibres to eFEX & jFEX
  - 6: Fanout requirements of EM ribbons to eFEX & jFEX
  - 7: Ditto for hadronic ribbons to eFEX & jFEX
  - 8: Layout of eFEX
  - 9: Layout of jFEX
  - (Ignore obsolete "OldRibbons" worksheet)