Optical Patch Panel

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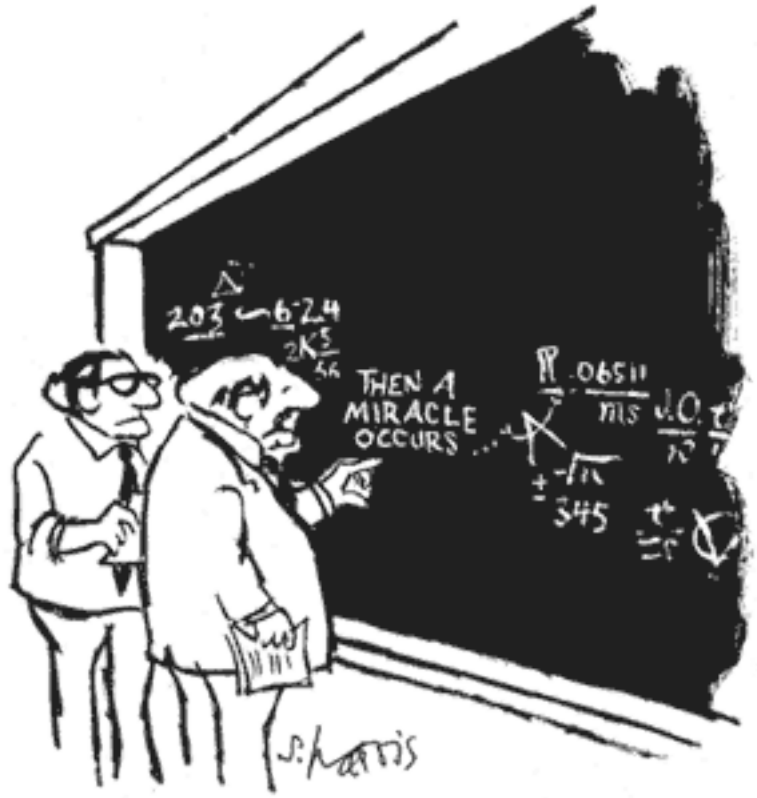
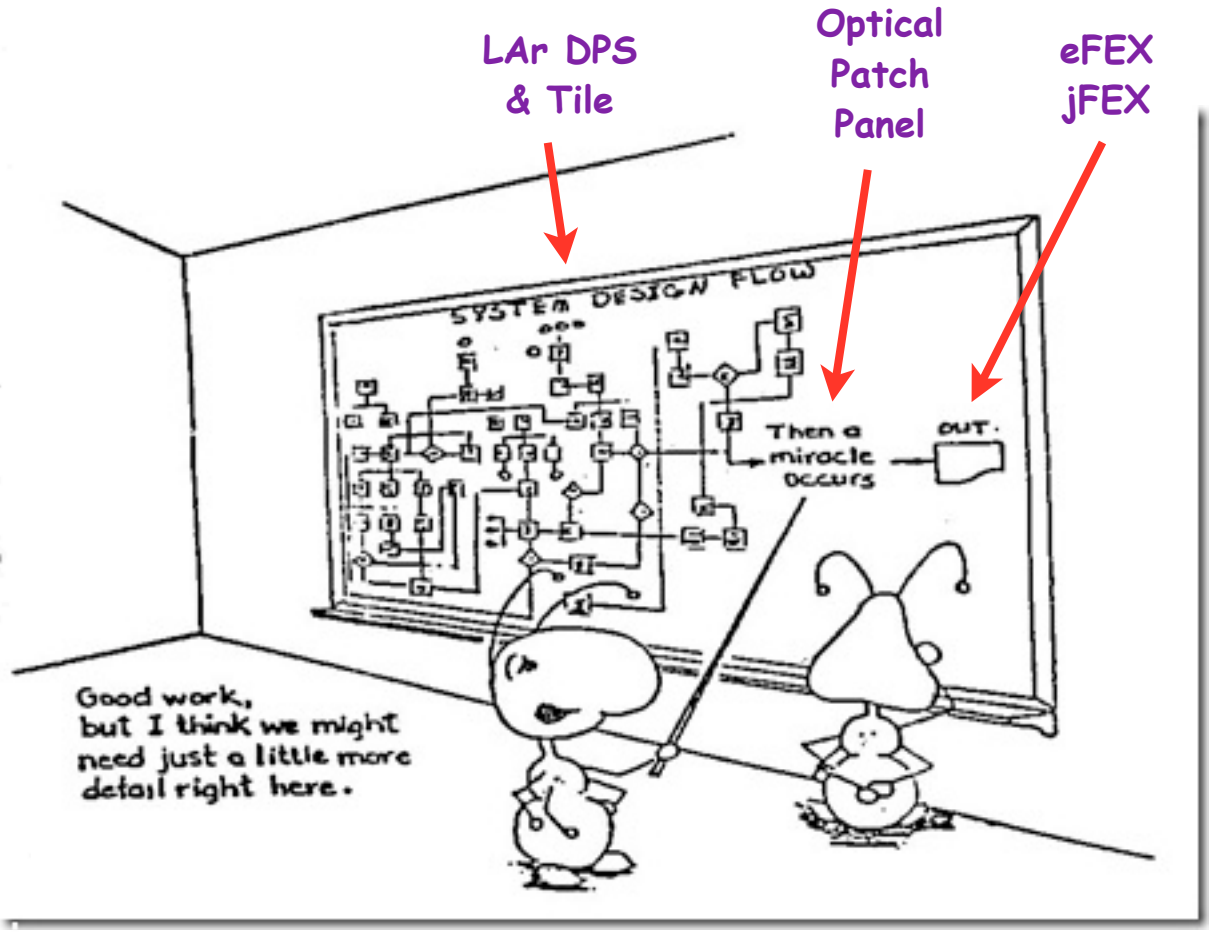
- Q: Is the optical patch panel viable?
- A: Maybe!

(My) Understanding Until Now...



"I THINK YOU SHOULD BE MORE EXPLICIT HERE IN STEP TWO."

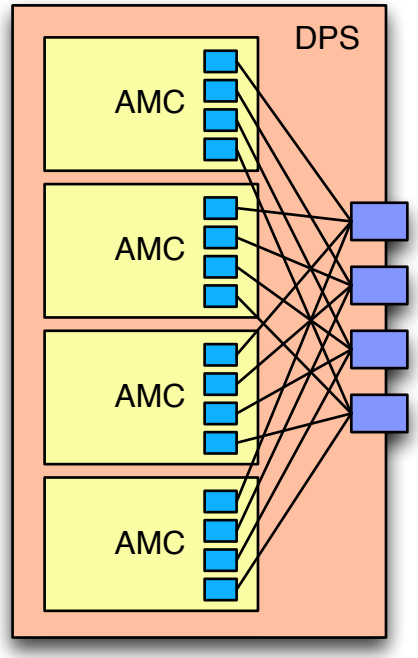


Aims and Assumptions

- Aims (conflicting!?)
  - Minimize number of optical connectors en route
  - Keep patch panel objects as simple as possible
  - Limited rack space: minimize size of optical plant
  - Tile inputs will change in phase 2
    - Different organisation of fibres in ribbons and/or different grouping of ribbons in multiribbon bundles
    - Avoid linking Tile PP (and Tile FEX inputs) with others
- Assumptions
  - 48-way (or 72-way) connectors can be split into four or more (up to 12) 12-fibre ribbons with any desired mapping
  - EM barrel/endcap overlap region handled by DPS
  - eFEX modules shifted by 0.4 in phi vs DPS boundaries
    - Optimise Tile/HEC overlap fibres

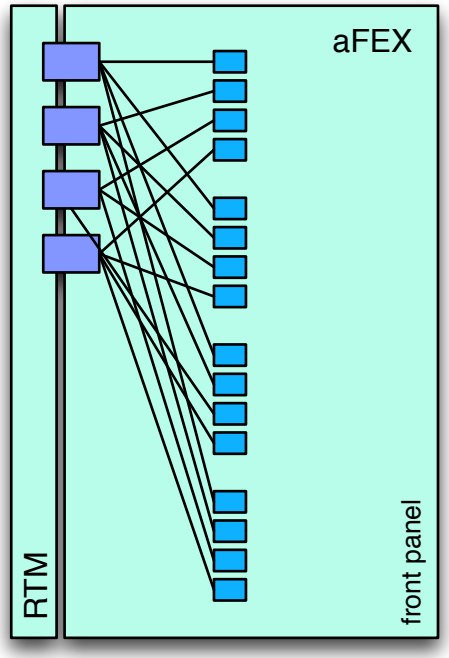
DPS Outputs

- DPS has four AMCs each with 4 micropods
  - Total of 16 * 12 fibre ribbons output
    - NB DPS also has similar number of fibres input
    - All inputs and outputs via front panel
  - Up to L1Calo to specify the output connectivity
  - Group outputs into four 48 fibre connectors?
    - Maybe front panel space for eight 24 fibre connectors??
  - Merge same AMC outputs to one connector
    - Group outputs by destination function
      - Not by source eta*phi
    - Aim for same AMC to DPS output mapping for all DPS
      - Including EMEC inner wheel, HEC and FCAL
        - Unless these regions also need special configuration of input optics
      - Easier for spares/maintenance
      - May require special firmware loads for EMEC-inner/HEC/FCAL (but thats probably required by the input mapping anyway)



FEX Inputs

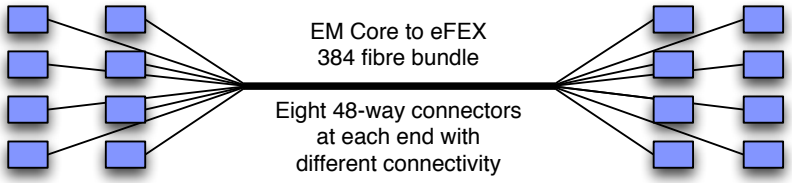
- Four 48 or 72-way input connectors
  - Via RTM and backplane zone 3
  - RTM currently seen as purely mechanical
- Pigtails to mini/micropods on motherboard
  - Mapping to suit board designers

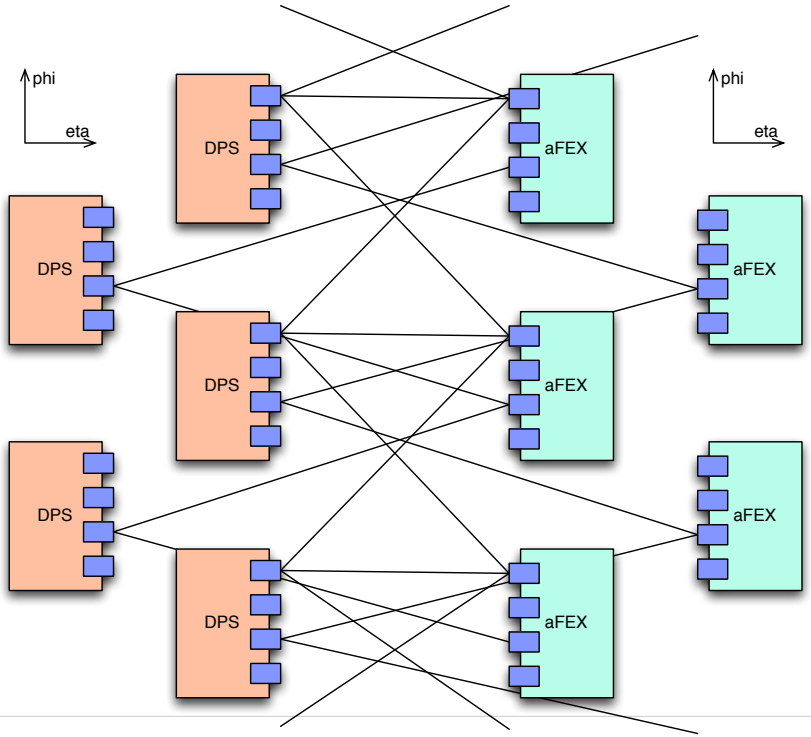


- Minimal set of optical connectors:
  - Source DPS AMC micropod
  - DPS front panel output
  - FEX backplane input
  - Receiving FEX mini/micropod
- How many more in the optical plant?

No Extra Optical Connectors!??

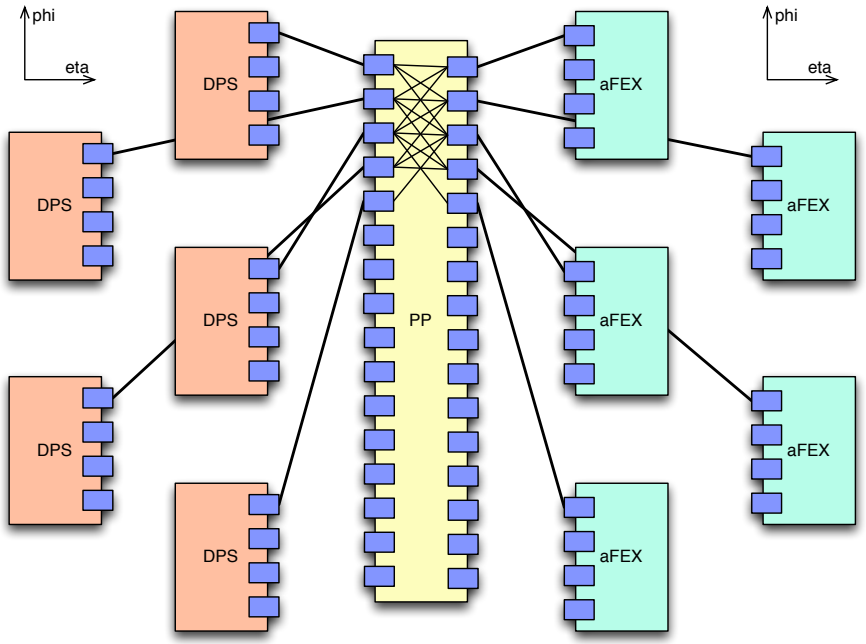
- Octopus bundles directly connecting input to outputs?
  - Fanout in phi (and eFEX corners)
  - DPS and FEX modules connected in both eta and phi
    - Especially eFEX with its &#**@% corners
  - Need hugely complex cylindrical woven tapestry of links
  - Small number of very complex cables
    - eFEX EM core: 6 of 2 or 3 types
      - 392 fibre bundle, 8*48-way each end
    - eFEX EM env: single object!?
      - ~1200 fibres, 24*48-way each end
    - eFEX hadronic: also single object?
    - jFEX like eFEX core?
  - Seems very impractical!





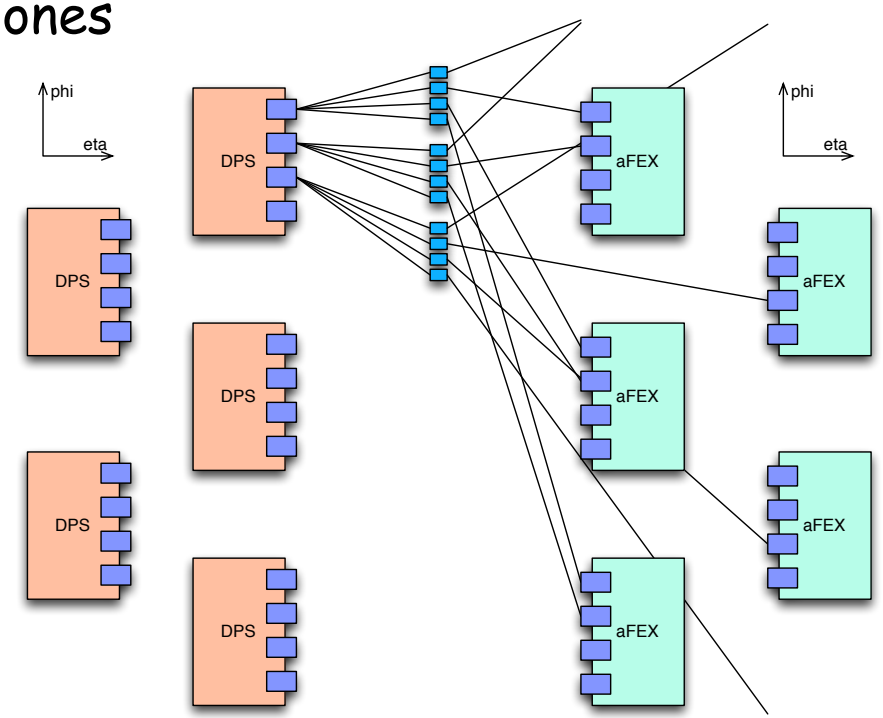
Two Intermediate Connectors

- DPS/FEX output/input bundles direct to PP object(s)
  - Possibly a little splitting into pigtails in awkward regions
    - But otherwise 48 way (or more) fibre bundles
  - Roughly same as previous slide but complexity is in boxes
  - Again probably very hard to make, small numbers, spares, etc
  - Pro: not laid in cable tray
  - Con: two extra connectors
  - Still seems impractical



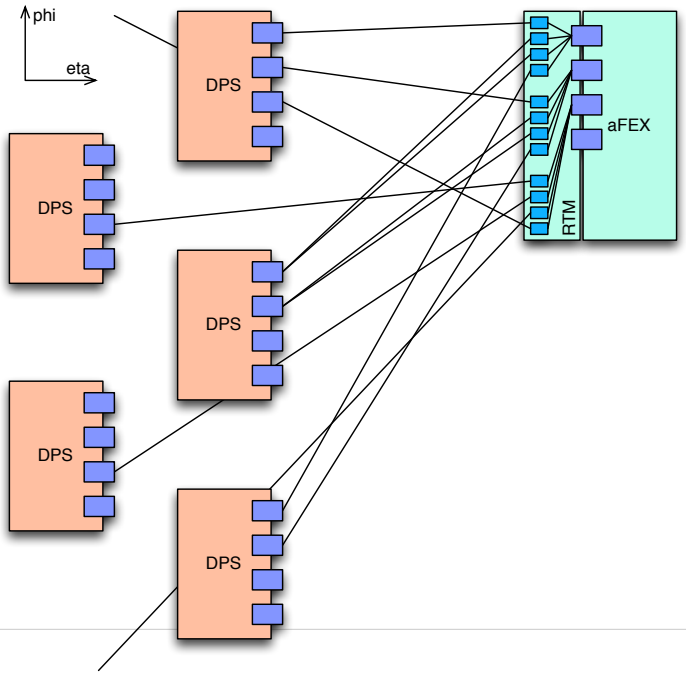
One Intermediate Connector (1)

- DPS 48-way outputs split into 12-fibre pigtails
- FEX 48-way inputs split into 12-fibre pigtails
- Connectors between pigtails
  - Result: nest of flying pigtails
  - More exposed fibres - fragile?
    - But not too hard to replace broken ones
  - Rough numbers
    - eFEX EM core: 96 of 2 or 3 types
    - eFEX EM env: 24 of 1 or 2 types
    - eFEX hadronic: similar
    - jFEX: 8 or 16 of a few types?
      - Many 12-fibre ribbons half used or less
    - Few each of a few types for:
      - HEC, FCAL, EMEC inner wheel



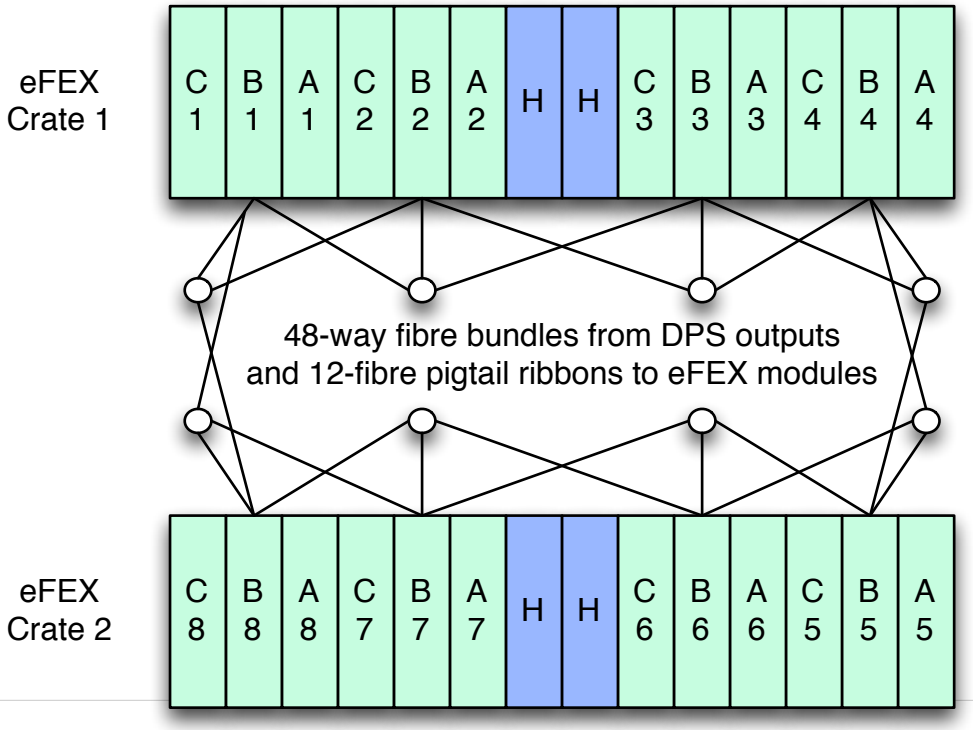
One Intermediate Connector (2)

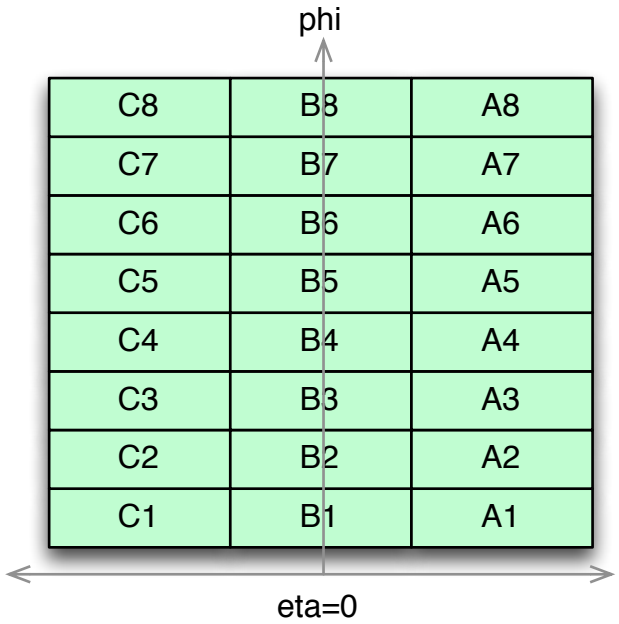
- Can we put the intermediate connectors on the RTMs?
  - At least some of them (preferably all)
  - If so, patch panel (or some of it) is part of the RTM
    - => Responsibility?
  - Pigtail spaghetti mostly hidden at the back of FEX racks
    - Possibly reduce number of racks needed for DPS+FEX systems
      - NB separate patch panels would have to be in lower part of racks
        - Underneath air deflectors
        - Best place for being kicked!
  - Feasibility?
    - eFEX: ~20 ribbons (12 EM, 8 had)
    - jFEX: ~40 ribbons??
      - May be reducible? [Two RTM-PP types with ~30]
    - RTM: 7cm deep, ~35cm high, ~3cm wide
    - Connectors: ~1cm??
      - Is there space for 20? Or 40??
    - Bending radius for fibres??



Rack and Crate Layout

- Pigtail connections between multiple eFEX modules
- Some 48-way bundles will connect to two crates
  - Both eFEX crates in the same rack
- Arrange eFEX modules in crates around in phi?
  - Pigtails go to RTMs in similar slots in upper/lower crates

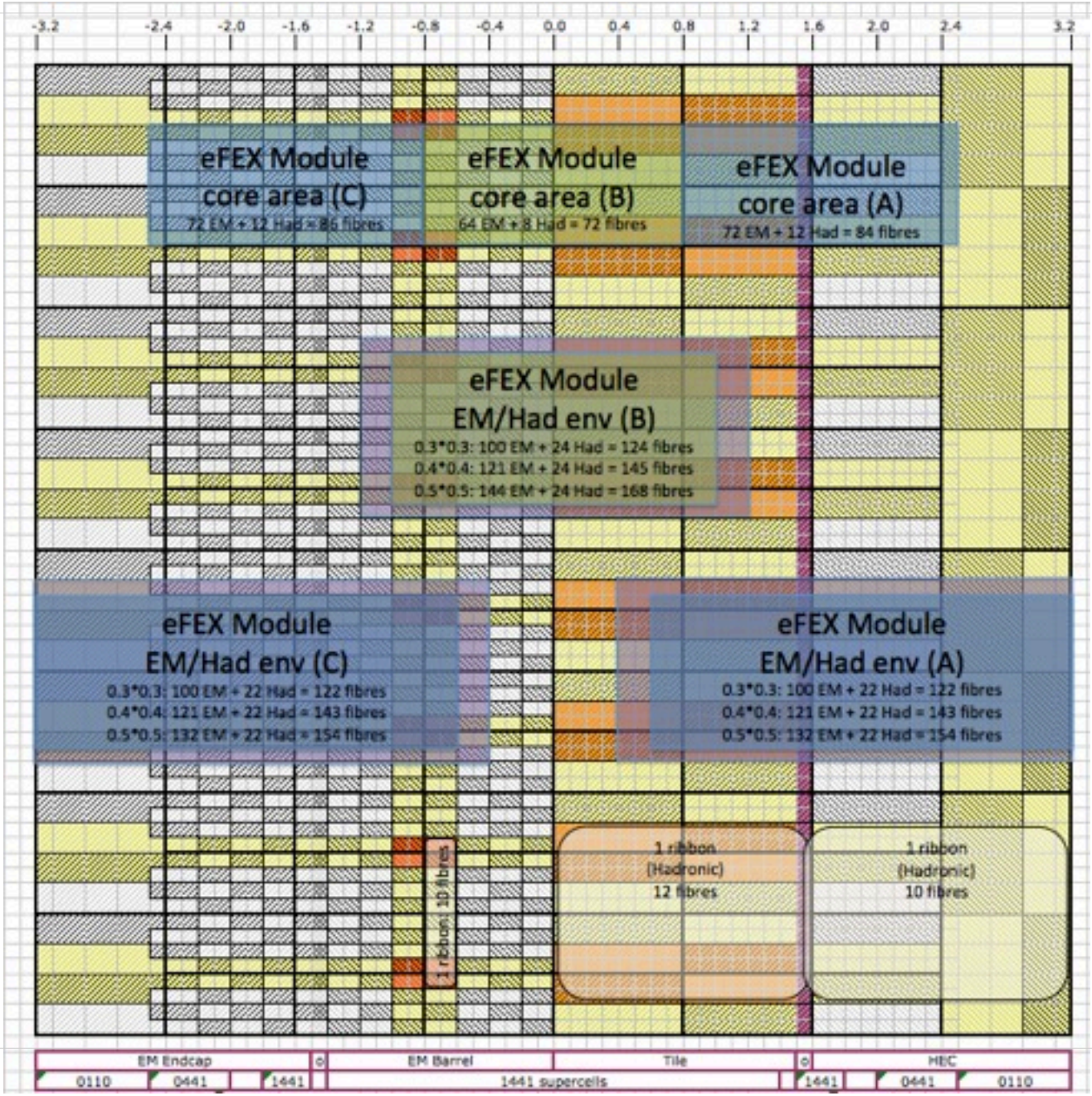


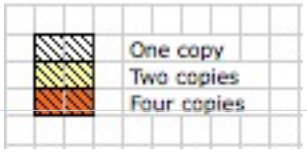


eFEX modules in eta*phi space

eFEX Layout (10 Gbit/s)

- Left: EM inputs
- Right: hadronic
  - NB slightly fewer hadronic fibres @ 10 Gbit/s
- Overlays:
  - Core region
  - EM & hadronic environments

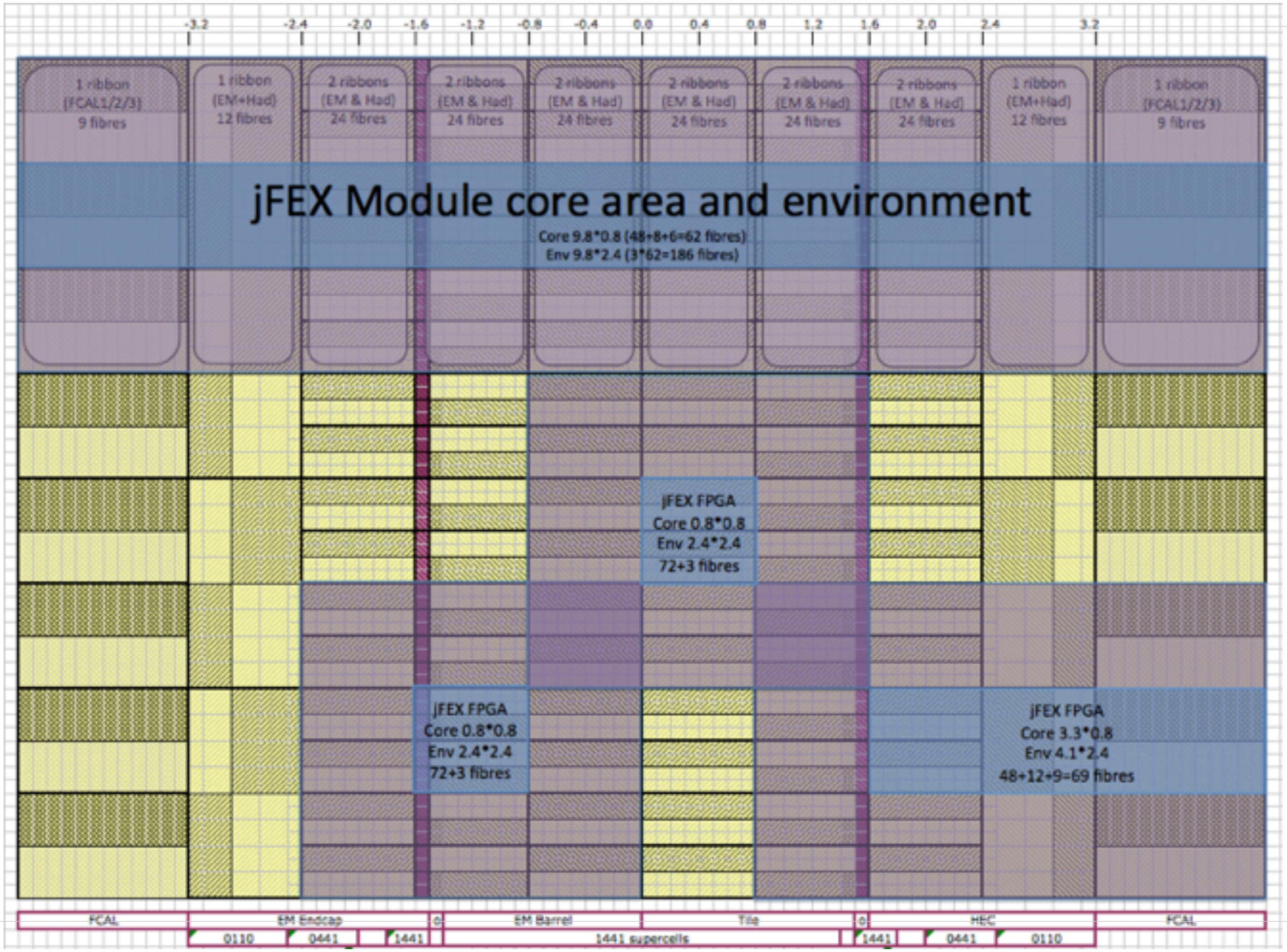




jFEX Layout (10 Gbit/s)

Version with six 80 input FPGAs allowing 1.7*1.7 size jets

Uli is considering version with four 96 input FPGAs

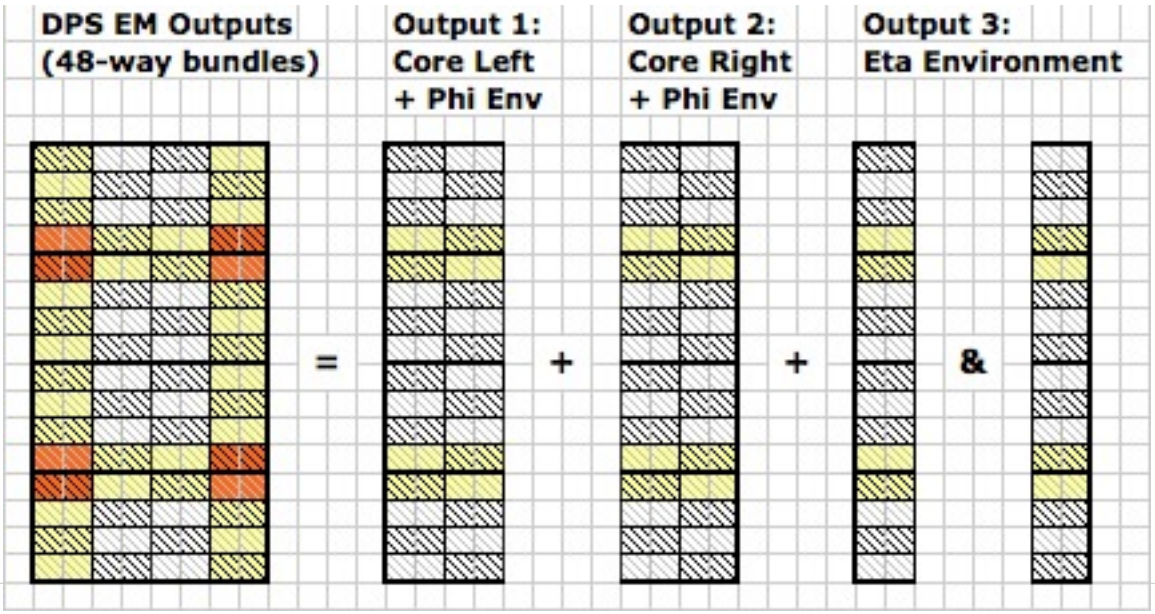


DPS Module Outputs

- Possible use of the four 48 way outputs per DPS
  - Entries with * need extra passive optical splitting
  - NB different HEC mapping at 10 Gbit/s cf 6.4 (Q: can it be combined with EMEC inner???)

System	EM central	EMEC inner wheel	HEC@6.4	HEC@10	FCAL
Output 1	eFEX (core left + phi env)	eFEX (core + env)	eFEX*	eFEX	jFEX
Output 2	eFEX (core right + phi env)	eFEX (core + env)	eFEX*	eFEX	jFEX
Output 3	eFEX (eta environment)	Unused?	jFEX*	jFEX	jFEX
Output 4	jFEX	jFEX	jFEX*	jFEX*	jFEX
N.DPS	24	2?	2?	2?	1?

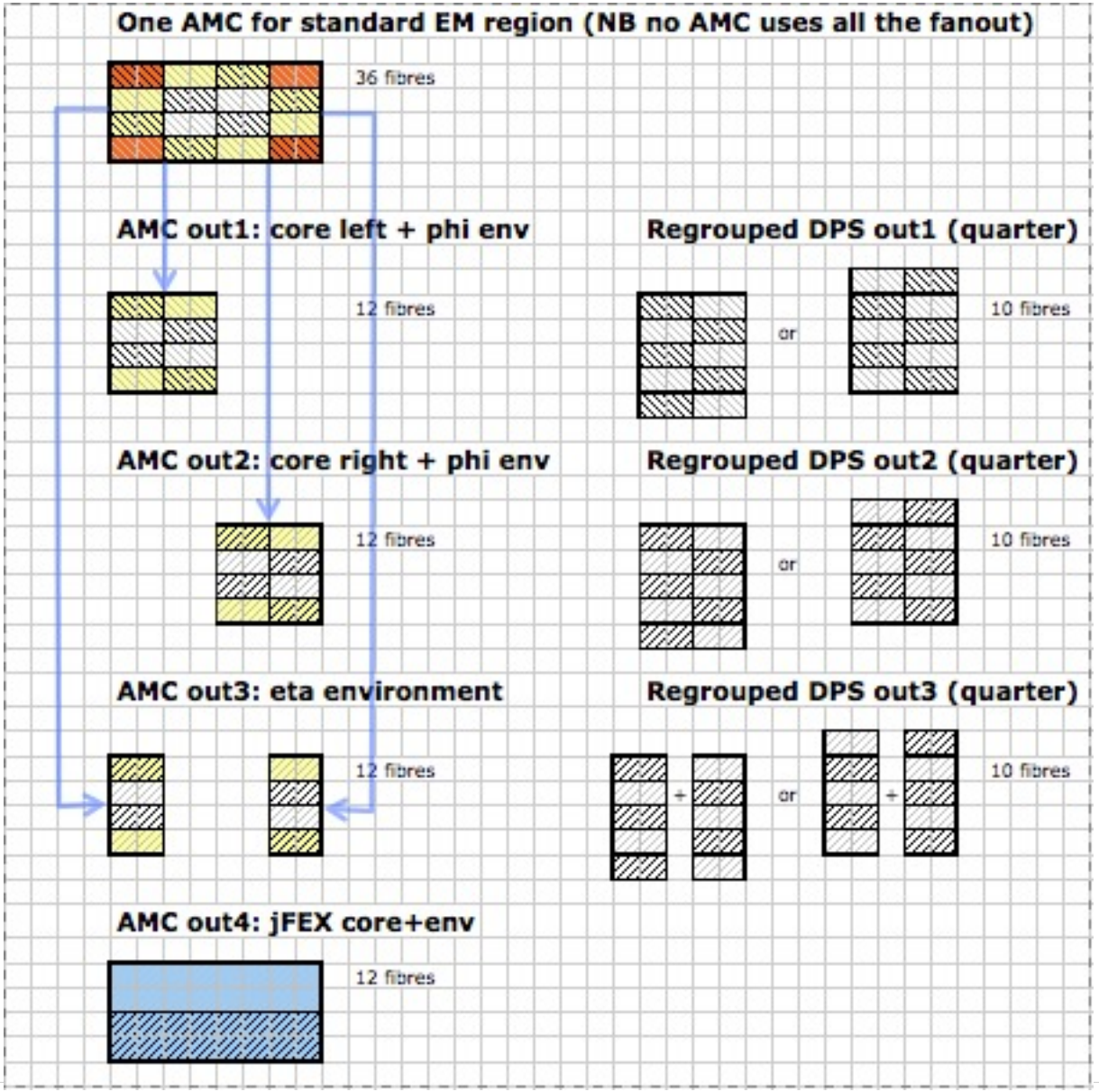
DPS Module (Standard EM region) covers 0.8*1.6 in eta*phi. Each AMC covers 0.8*0.4



+ Output4: jFEX

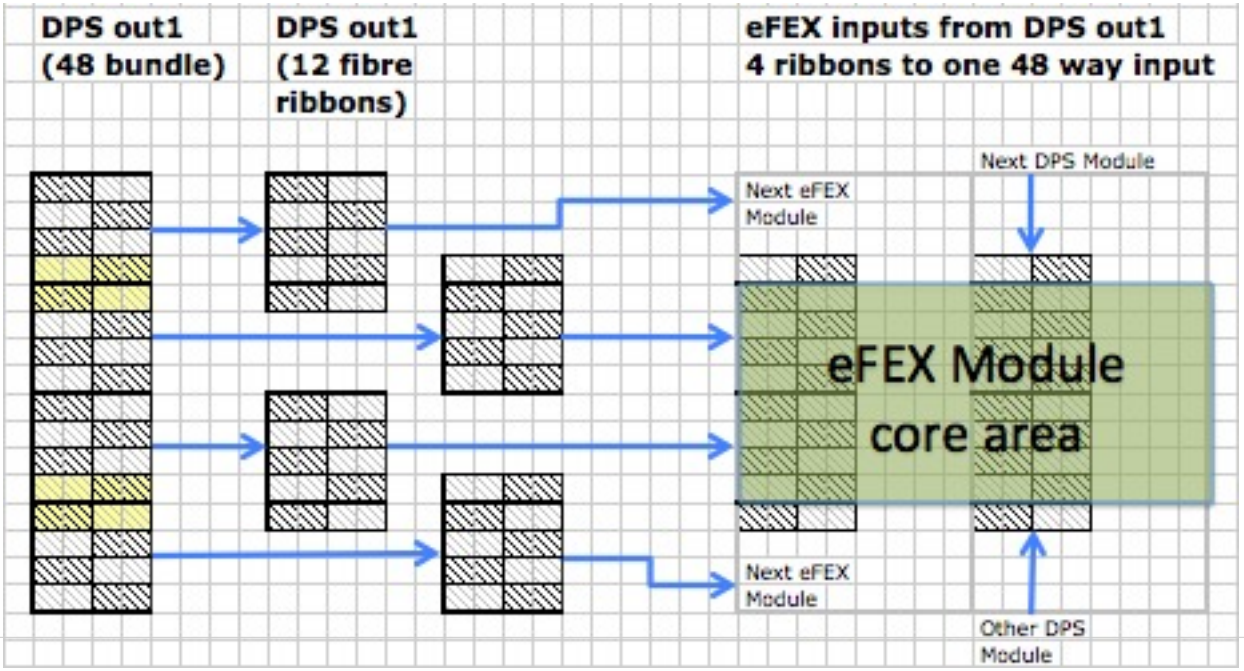
Outputs from DPS AMC (EM)

- Standard EM region
  - 1: eFEX core left + phi environment
  - 2: eFEX core right + phi environment
  - 3: eFEX eta environment
  - 4: jFEX core + environment
  - NB phi environments need regrouping to other ribbons at DPS outputs



EM DPS Output 1 (Core Left)

- Four 12-fibre ribbons from AMC output1
- Grouped into 48-way connector on DPS
- DPS output regrouped into four different ribbons
  - Connected to three different eFEX modules
- Combine phi environment with neighbouring core area



Summary

- Tried to look at optical patch panel details
  - Mainly considered EM inputs to eFEX
    - Some work on jFEX and hadronic inputs to eFEX
    - Completely ignored possible gFEX
  - Favour "nest of flying pigtails" approach?
  - Favour merging patch panel with FEX RTMs?

- Next steps?
  - Responsibility implications if RTM merged with patch panel?
  - If OK with L1Calo, check scheme with LAr
  - Work out more details (especially Tile @ phase 1 & 2)
  - Document...

Backup Notes

Backup Notes: Tile Inputs

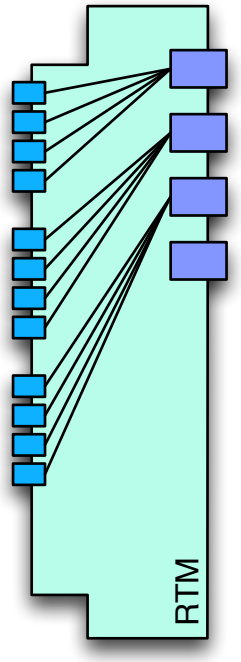
- Phase1/LS2/Run3
  - Does JEM have single 48-way output connector? Check!
    - Split into 8 pigtails, only 3 fibres used per 12-fibre ribbon
- Phase2/LS3/Run4
  - Tile ROD probably 3.2*0.2 in eta*phi
    - If so, alternate pairs of RODs in phi need more or less fanout to eFEX
      - RODs covering 1.6*0.4 could all have same number of used outputs
  - Single 48-way output connector OK (at 10 Gbit/s)
    - Split into 3 (or 6) pigtails (4,8,4 fibres used per ribbon)
- FEX RTMs
  - Different pigtail configuration for Tile phase1 & phase2

Backup Notes: RTM Types

- Single RTM configuration for jFEX (in principle)
  - However two different configurations for alternate jFEX modules in phi would allow fewer connectors in total
    - Have 1.6+0.8 or 0.8+1.6 in phi vs regular 3*0.8
  - Alternate way of reducing number of connectors would be to have different mappings in firmware for alternate jFEX modules
- Three (two?) configurations for eFEX
  - C side, Barrel and A-Side
  - Single type for C-side & A-side with reflection in firmware??

Backup Notes: RTM Size

- Is 7cm RTM depth enough for bending radius?
- If not, is it possible to have extended front panel?



Backup Notes: HEC+EMEC Inner

- At 10 Gbit/s only one HEC DPS output needs to be split
- While EMEC inner wheel DPS has one unused output
- Can HEC and EMEC inner wheel DPSes be combined?
  - Combination required at the AMC FPGA level
  - Half EMEC LTDB + half HEC LTDB to same AMC
  - If so, maybe no need for passive optical splitting anywhere!