Phase 1 Tile Inputs @ 10 Gbit/s

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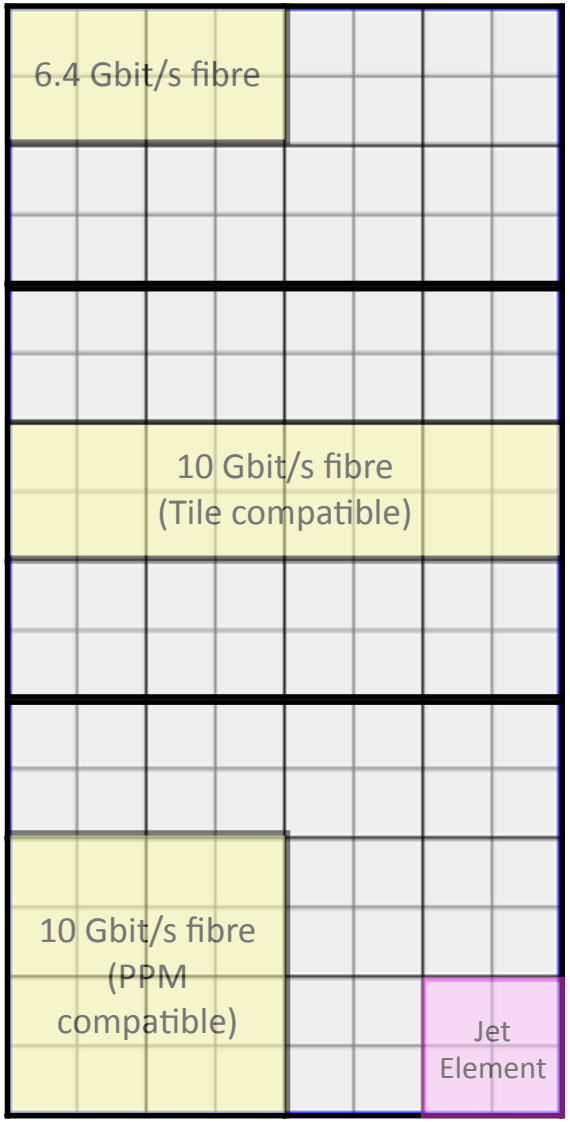
- Tile input baseline and fallback
- Impact of moving to 10 Gbit/s

Tile Input Baseline and Fallback

- Baseline choice via JEMs
  - Tile inputs at phase 1 (post LS2, Run 3) via three (of 4) JEM input modules
  - Irregular phi coverage (due to phi fanout): 0.8*0.4, 0.8*0.6, 0.8*0.6
  - 6.4 Gbit/s fibre: 8 towers as 0.4*0.2
  - 10 Gbit/s fibre: 16 towers as 0.8*0.2 to be compatible with Tile phase 2 ROD
    - Expected to cover 3.2*0.2 in eta*phi
- Fallback option via PPMs
  - But 10 Gbit/s fibre cannot be 0.8*0.2
- Good to test JEM route early
  - Otherwise mappings may need to change with impact on Tile phase 2 ROD



JEM core: 0.8*1.6 in eta*phi