# Notes from LAr Upgrade WG4

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- Front end: not sampling at the peak?
- Busy cables -> fibres?
- Connection to DCS
- Readout to TDAQ
- Basic mappings

- And they also need decisions on mappings...

# LAr Upgrade Working Groups

- Several working groups established by LAr
  - First to prepare the IDR, now to prepare the TDR
  - Three each for front and back end systems
    - WG1: analogue signals
    - WG2: LTDB digital side
    - WG3: LTDB (front end) global issues
    - WG4: LDPS (back end) global issues
    - WG5: LDPS hardware
    - WG6: LDPS firmware
  - Both LAr and TDAQ IDRs encourage communication
    - I got asked to join WG4 a few months ago
    - So far I only managed to attend a couple of vidyo meetings
  - WG agenda pages at:
    - https://indico.cern.ch/categoryDisplay.py?categId=3283

# Notes from LAr WG4 (1)

- LAr propose NOT to sample at the peak of the pulse
  - Sample at random phase with no clock delays on the LTDB
  - Studies of filters by Arno&co in Dresden => should be OK
  - Are we happy with this?
    - NB I havent seen these results
  - Background: LAr plan to use GBTx to control the LTDBs
    - One (or maybe two) GBTx per quarter LTDB
    - Each GBTx has 49 clock outputs, only 8 with programmable phase
    - Need clocks for each 4-channel ADC (20) and serialiser (5 or 20)
      - N. clocks per serialiser depend on using custom LOCx2 (5) or GBTx (20)
    - Sampling at the peak would require rethink of LTDB clocking scheme...

# Notes from LAr WG4 (2)

- LAr thinking of sending ROD Busy via fibre
  - Then have to convert to electrical for ROD Busy module
    - If LAr do this, would we want to go the same route?
- Connection to DCS
  - Some kind of "system manager" above shelf managers
    - Only system manager would communicate to DCS
    - IPMC board only for single board control, not the whole crate
      - NB will L1Topo use the LAPP IPMC card?
- Readout to TDAQ
  - LAr still has an open question **whether** to read out to TDAQ
    - Or just for local monitoring purposes (not synchronised with L1Calo)
  - Ive told them we would certainly like some readout each L1A!
    - My feeling is that at least we need the filter output each L1A
      - And ideally the option to send ADC samples to cross check filters
    - But it all needs a bandwidth estimate and OK from TDAQ
      - Roughly 40k supercells, how much compression?

# Notes from LAr WG4 (3)

- Mappings (my understanding/guesswork @ 6.4 Gbit/s)
  - Working assumption: DPS EM FPGA covers 0.8*0.4 in eta*phi
    - With HEC probably one quadrant of one side, ie 1.7*1.6
      - And only two copies of HEC towers (of four required)
  - DPS FPGA will have 4 * 12 fibre ribbons out
    - EM
      - One ribbon using 10 fibres: 2*jFEX (0.4*0.2) + 8*eFEX (0.2*0.1)
        - Could orient eFEX and/or jFEX along phi instead of eta
      - Two ribbons covers 0.8*0.4 (single copy)
      - NB two spare fibres per ribbon, might be usable for extra copies for eFEX corners
        - Multiple configurations: we may need to ask very nicely!
    - HEC
      - Need all 12 fibres to cover 1.7*0.8 (single copy)
      - All 48 output fibres for two copies of entire quadrant
        - Need extra splitting to get the required four copies for 2*eFEX + 2*jFEX
        - Nothing to spare for eFEX corners => additional optical splitting
    - FCAL
      - Need 12 fibres for 0.8 in phi at each end (two copies)
        - OK since we (presumably) do not want FCAL for the eFEX

# Notes from LAr WG4 (4)

- Content of links
  - Assumptions by LAr (IDR)
    - eFEX:Two towers (20 supercells) BCMUXed into one fibre
      - 10 bits per supercell plus 1 bit BCMUX => 110 bits per BC per fibre
      - Leaves 18 spare bits => extra dynamic range, timing, quality, checksums?
    - jFEX: 8 0.1*0.1 towers on one fibre
      - 12 bits per tower => 96 bits per BC per fibre
      - Plus sumE (n.bits=16?)
      - Leaves some spare bits: extra dynamic range, Ex&Ey, checksums?
  - FPGAs at both ends so can keep some flexibility
    - But good to have an agreed baseline