Notes from LAr Working Group

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- Mapping discussions & questions
- Fanout pattern slide shown to LAr

Mapping discussions with LAr

- New LAr working group for mappings document
  - Few people from LAr front & back end groups
- I prepared various spreadsheets
  - Mainly for myself to understand issues & fanout requirements
    - Which have changed because of the new eFEX and jFEX baselines
  - Shown to LAr with a short talk to try and explain it to them...
  - Phone meeting yesterday (talk & spreadsheet available here):
    - https://indico.cern.ch/conferenceDisplay.py?confId=249111
  - They will go away and cogitate my proposals & questions
- Some issues and questions
  - Can we handle mappings that are reflected in eta & phi?
  - jFEX retransmission fanout => inputs not all synchronised
    - Personally I prefer all fanout (incl at eta=0) at source or by splitting
  - New question: bandwidth/mapping implications of Tile D cells??

LAr (Mapping) Progress

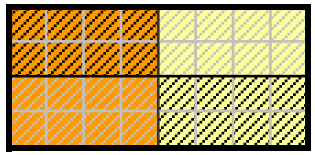
- Front end crate
  - Backplane designs for EM Barrel and standard EM Endcap
  - Not yet done for EM overlap, inner wheel, HEC or FCAL
- FE to DPS
  - No details yet
- DPS internals
  - No details yet
- Basically working inwards from FE & L1Calo to DPS…

Fanout Patterns from DPS

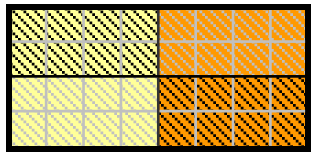
- Can one DPS fanout pattern handle corners?
  - New eFEX baseline no longer needs 2 copies of all fibres
  - But needs four copies in some places
  - New jFEX baseline needs four copies around eta=0
    - jFEX has a possible solution, but fanout at source would be better
- Suggested patterns (see spreadsheet for details)
  - One 36 fibre pattern covers all eFEX cases
    - No DPS FPGA needs to enable all outputs
  - Need two patterns for jFEX (or one reflected at eta=0)

36 fibres

eFEX outputs
1, 2 or 4 copies



12 fibres



12 fibres

jFEX outputs
2 copies everwhere
(except 4 at eta=0)