Ultra Preliminary DPS-FEX Mappings

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- Overview
- LAr FE Crate Layout
- Ideal Mapping for L1Calo??
- eFEX (and jFEX) Mappings
- Miscellaneous Notes

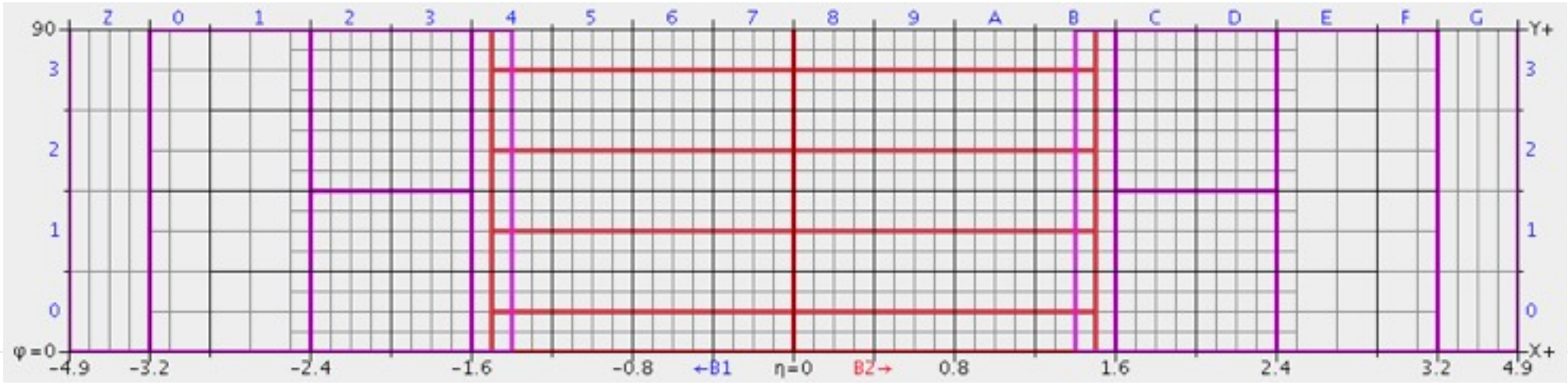
WARNING! Not yet agreed with LAr!
All mappings assume use of BCMUX!

Overview

- We will need detailed mappings for the TDR
  - These must be agreed with LAr - and be feasible!
- Start with mappings that might be ideal for L1Calo
  - And which might be possible based on discussions so far
    - Our aims have been discussed with LAr over one or two years
    - LAr designs for LTDB and LDPB have taken much on board
    - But the ideas have not been worked out in detail
  - Awkward areas may still cause problems => extra fibres!
- When its all agreed it should be documented in detail
  - For now, start with some slides...

Layout of LAr Front End Crates

- The diagram shows a phi quadrant of the EM layer
  - The faintest grey divisions are trigger towers
  - Outlines in red/purple are the barrel/endcap FE (whole) crates
    - Each crate is split into two half crates: one TBB and LTDB per half crate
    - The geometry is very different in barrel, overlap, endcap and high eta
    - There are clear boundaries at eta=0, |eta|=1.6 and |eta|=2.4
    - The overlap region is clearly going to be difficult...

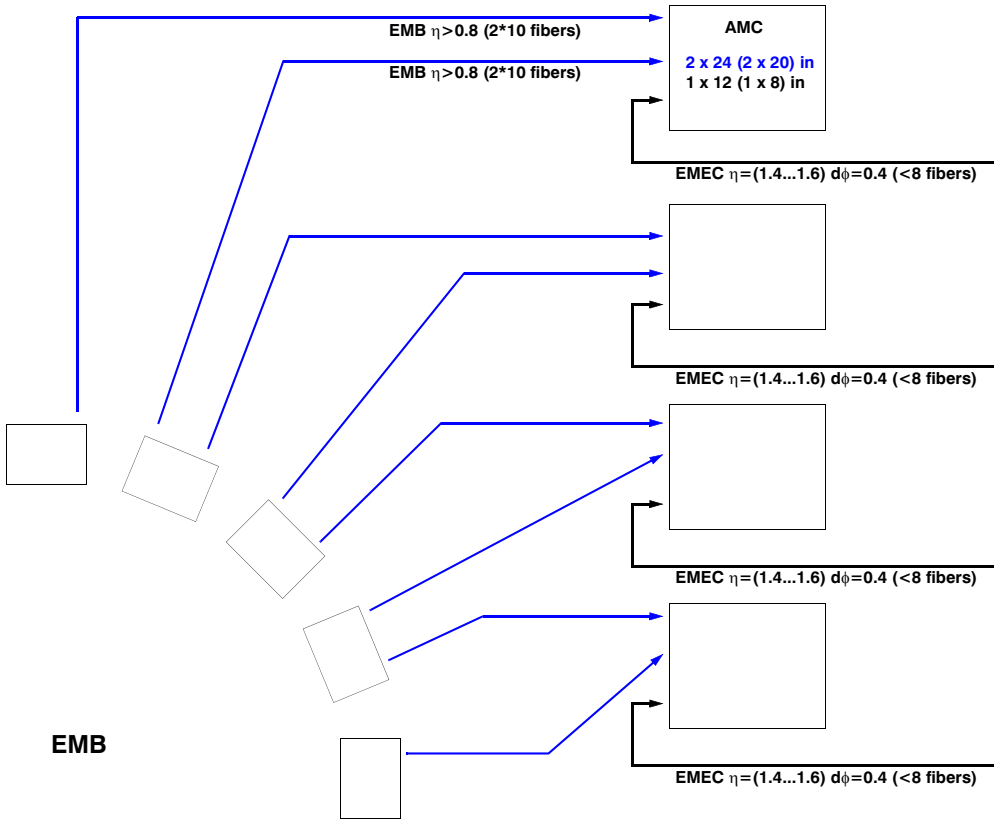


Baseline LAr Design

- Front end: LTDB
  - Handles 320 supercells
  - Complex mapping: minimise crossing backplane tracks
  - Regroup fibres onto ribbons with on board pigtails?
    - Presumably need different configurations in different regions?
- Back end: LDPS board (LDPB) has four mezzanines
  - One FPGA per mezzanine with 8 micropods (4 in, 4 out)
    - Total of 32 micropods per ATCA board
    - Challenging, but they think they can do it...
  - Four input ribbons per FPGA from (equivalent of) one LTDB
    - No remapping of fibres within ribbons between FE & BE
      - But can reorganise whole ribbons between LDPS inputs
      - Might (possibly) add extra ribbon connector to facilitate overlap????
  - Four output ribbons per FPGA to FEXes
    - 48 fibres output for 320 supercells (32 0.1*0.1 towers)

EM Overlap Region Sketch

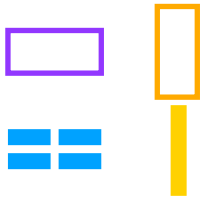
- Sketch for handling EM overlap region (Stefan Simion)
  - Depends on being able to patch ribbons going to the DPS…
    - If not, need one extra EM fibre for 1.4<|eta|<1.5 (0.1*0.4, 2*4 supercells)

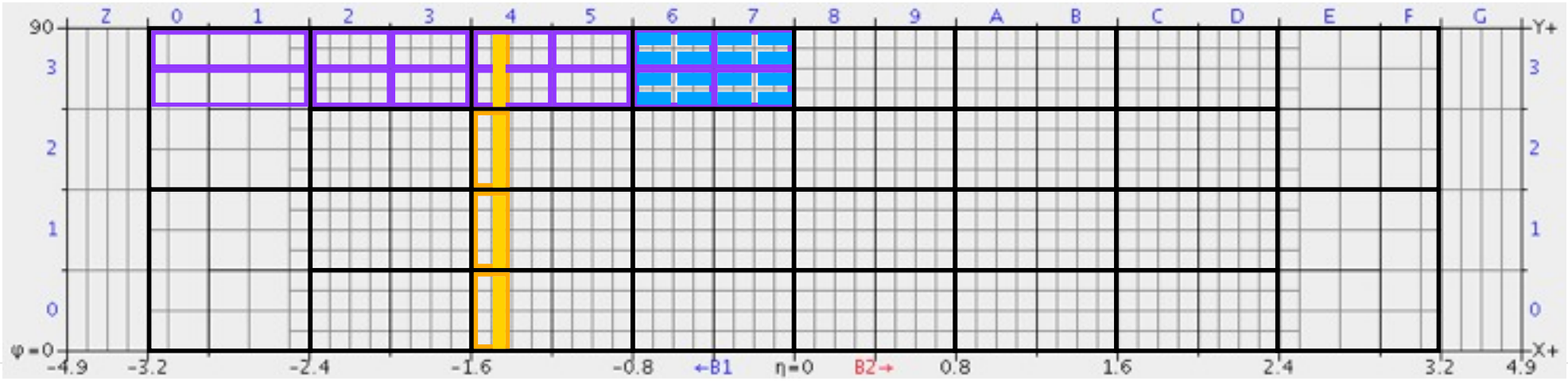


Ideal DPS FPGA Mapping: EM

- Aim to have each DPS EM FPGA cover a regular area
  - One FPGA can handle 32 towers (320 supercells)
  - Try for regular pattern of 0.4 * 0.8 in eta*phi
    - OK in endcap, probably in central barrel, challenge for overlap

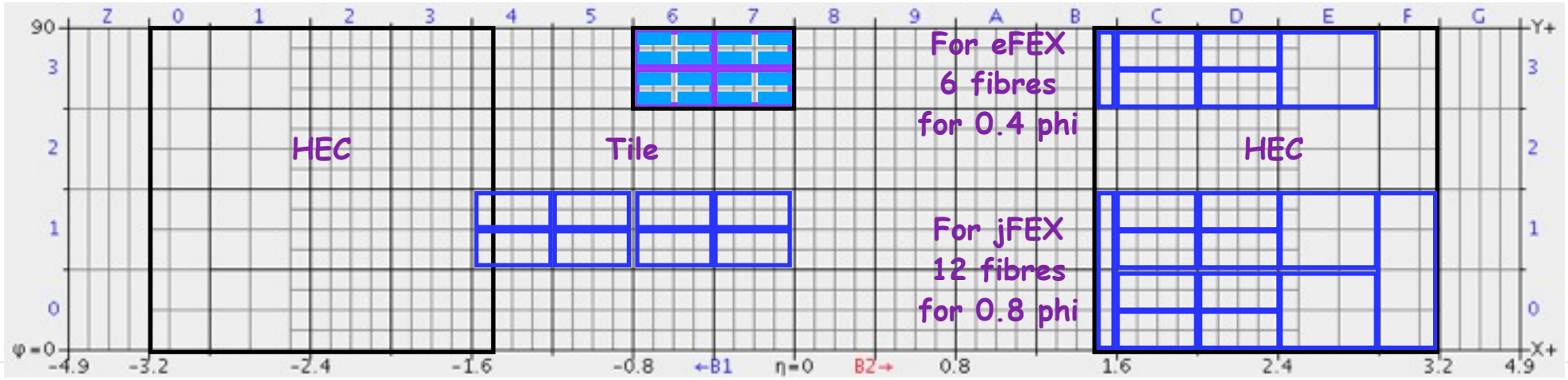
- Expected EM output fibres:
  - For jFEX: one fibre per 8 TT as 0.4*0.2
  - For eFEX: one (BCMUX!) fibre per 2 TT as 0.2*0.1
    - NB EM fibre 0.2 in eta is good for phi oriented eFEX
    - But may be hard in overlap region and not obvious for |eta|>2.4





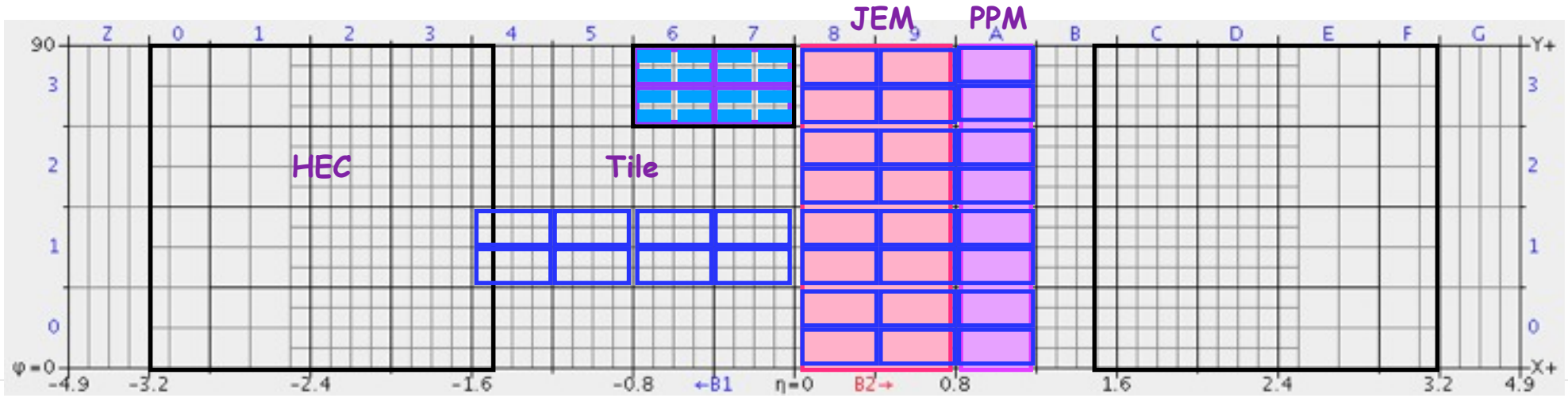
Ideal DPS FPGA Mapping: HEC

- HEC DPS Mezzanine: 1.5<|eta|<3.2 * 0.8 phi? (Check!)
  - One LTDB per quadrant per side: 16*10 + 8*4 = 192 towers
  - One fibre per 0.2*0.4 in eta*phi - where possible
    - But HEC starts at |eta|=1.5 and has slice at 2.4<|eta|<2.5
      - For jFEX have fibres containing 0.1*0.8 in eta*phi, for eFEX need just 0.4 in phi
      - For |eta|>2.5 we need fibres covering 0.4 in phi (no room/need for last two bins to eFEX)
      - Different mappings for eFEX and jFEX, underused fibre for eFEX at 1.5<|eta|<1.6
  - Total of 24 fibres for one copy: 48 fibres (max) for 2 copies
    - Need four copies (2*eFEX + 2*jFEX) => passive optical split
      - Or else use twice as many half full DPS mezzanines...



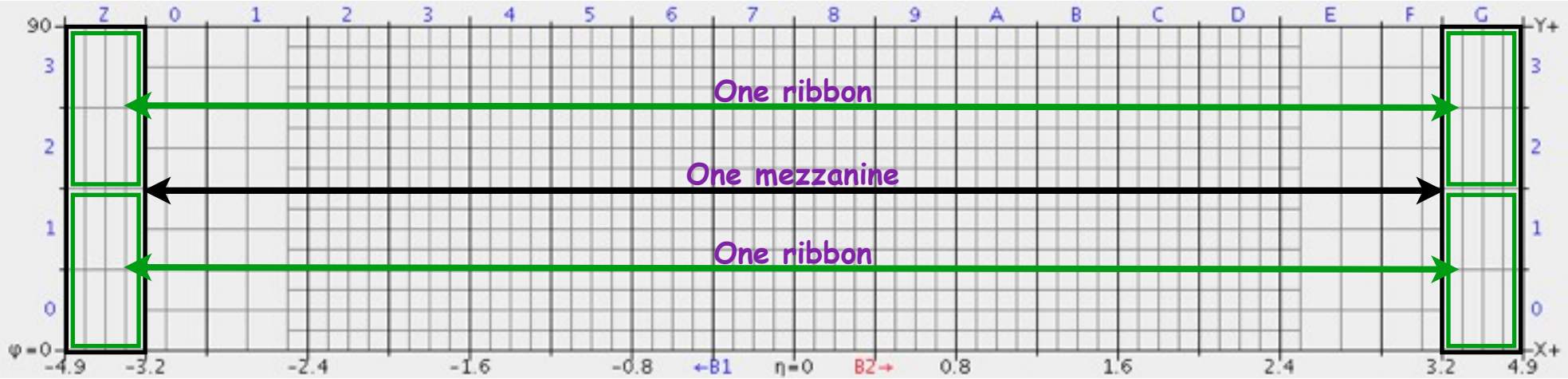
Ideal DPS FPGA Mapping: Tile

- Legacy phase 1 must be compatible with phase 2
  - One fibre per 0.2*0.4 in eta*phi
    - Matches current PPM/JEM
    - Should be compatible with proposed phase 2 Tile ROD
  - Four copies from PPM (or JEM) interface (2*eFEX + 2*jFEX)
    - Ignore HEC cells at 1.5<|eta|<1.6
      - For phase 2, split currently merged |eta|>1.4 Tile tower
      - Or add gap/crack scintillators?



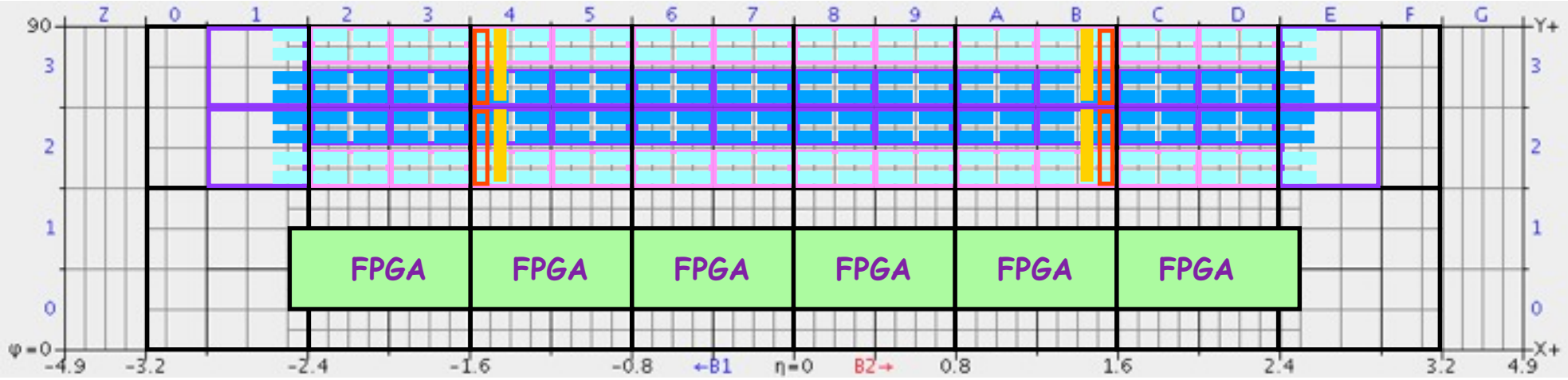
Ideal DPS FPGA Mapping: FCAL

- Consider phi oriented jFEX
  - Useful to have quadrant of FCAL A&C in one DPS mezzanine
    - (Avoids having to patch fibre ribbons afterwards)
    - Two LTDBs per side => half LTDB per quadrant per side
    - N. supercells per 0.4 in phi: FCAL1=12, FCAL2=8, FCAL3=4
    - Total 24 supercells per 0.4 phi per side => 3 fibres @ 8 SC/fibre
    - One ribbon covers 0.8 phi for both A and C sides all 3 layers
      - 24 fibres per quadrant, duplicated to 48 fibres



Mapping to eFEX Module (1)

- Assume two crate phi oriented eFEX design
  - 8 eFEX modules per crate, each handling 5.0*0.4 in eta*phi
  - The diagram shows the worst case for 0.5*0.5 environment
    - For 0.4*0.4, one row of EM fibres is removed
    - For 0.3*0.3, two rows of EM fibres and one hadronic are removed
      - The latter requires the core region to be shifted by 0.1 in phi (instead of 0.2 shift)
    - Duplicated fibres for environment fanout are shown in lighter colours
      - Possible additional fibres at boundaries are shown in yellow (EM) or orange (HEC)
    - Possible division between four (0.4*1.2) or six (0.4*0.8) FPGAs?
      - The two end FPGAs have less fan in but one extra phi bin of core processing



Mapping to eFEX Module (2)

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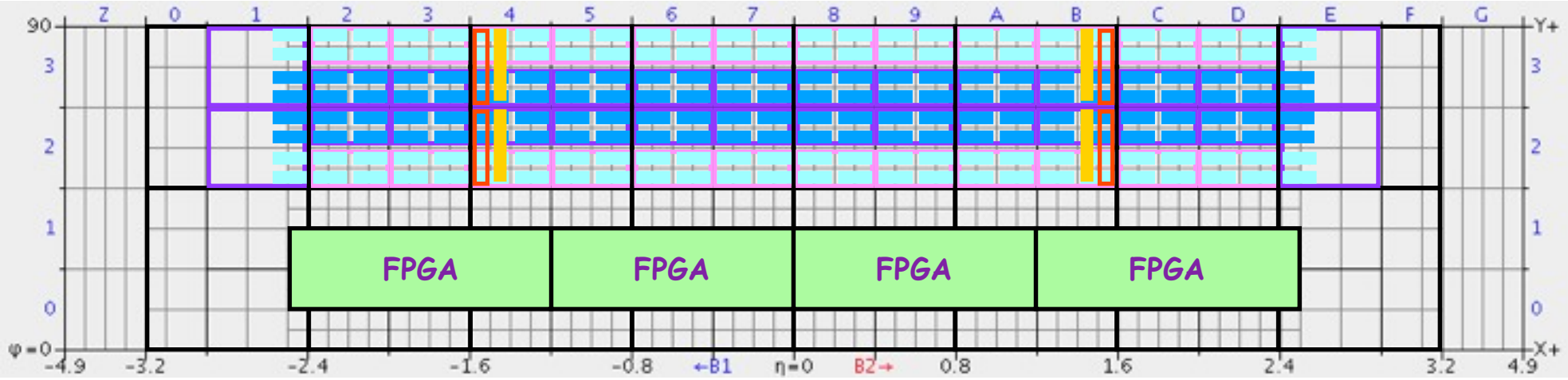
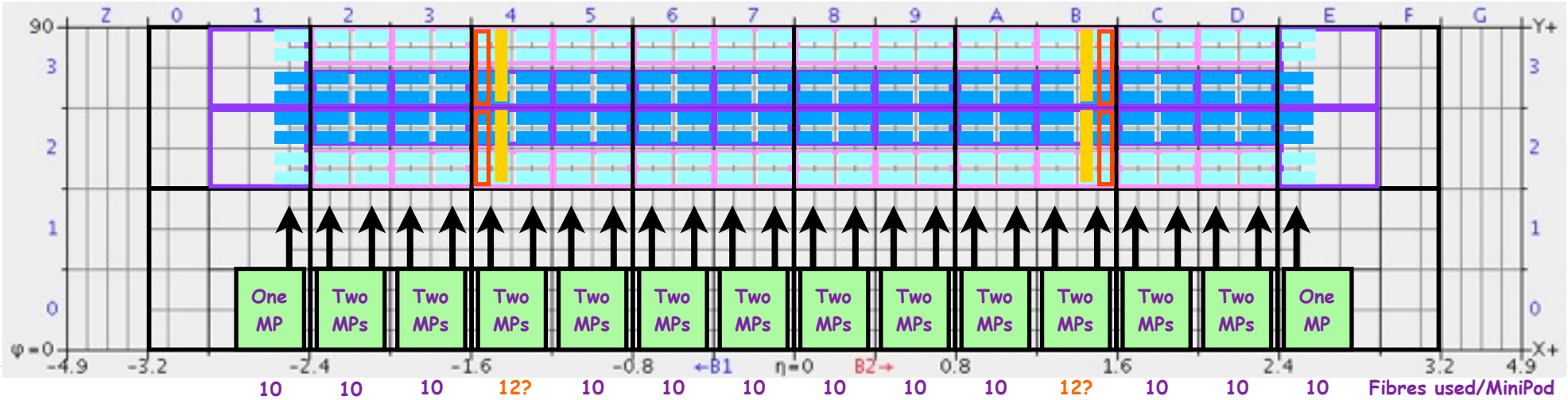


eFEX Fibre Ribbon Mapping

- Simplest: 2 ribbons (2 minipods) for 0.4 in eta
  - Most ribbons use only 10 of the 12 fibres (for 0.5*0.5 env)
    - Some ribbons may use 11 or 12 fibres at boundaries with same layout
  - More ribbons per module than a really compressed mapping
    - But regular mapping per FGPA => easier layout of the board??
    - Total of 26 ribbons (minipods) per module
      - Same layout could handle either 0.4*0.4 or 0.5*0.5
      - Need to track one less fibre per minipod in the 0.4*0.4 case
  - For 0.3*0.3 environment more compact mapping possible
    - But most obvious regular mapping has no spare fibres for boundaries



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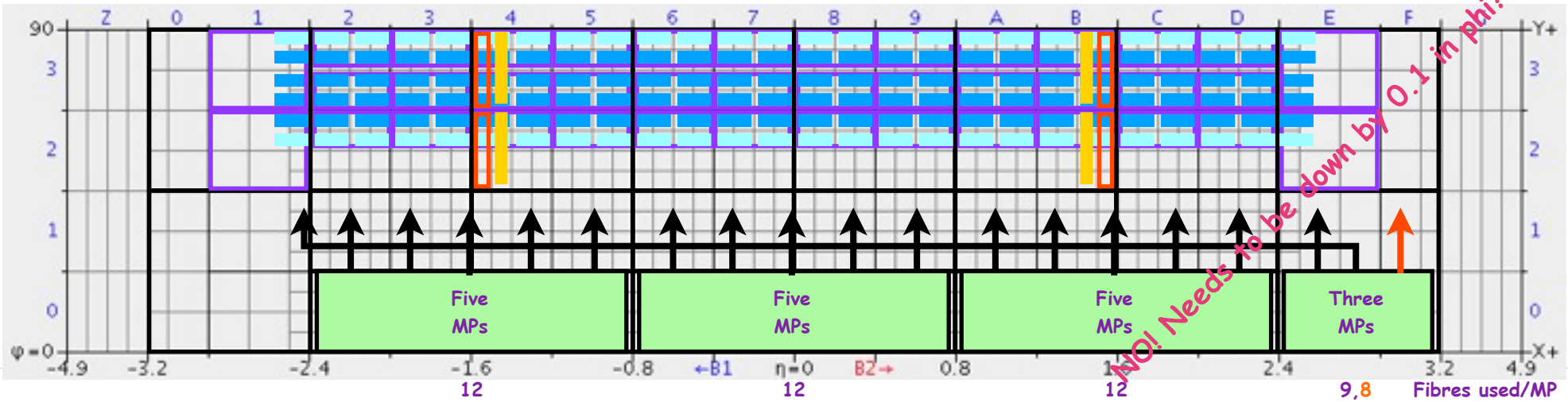
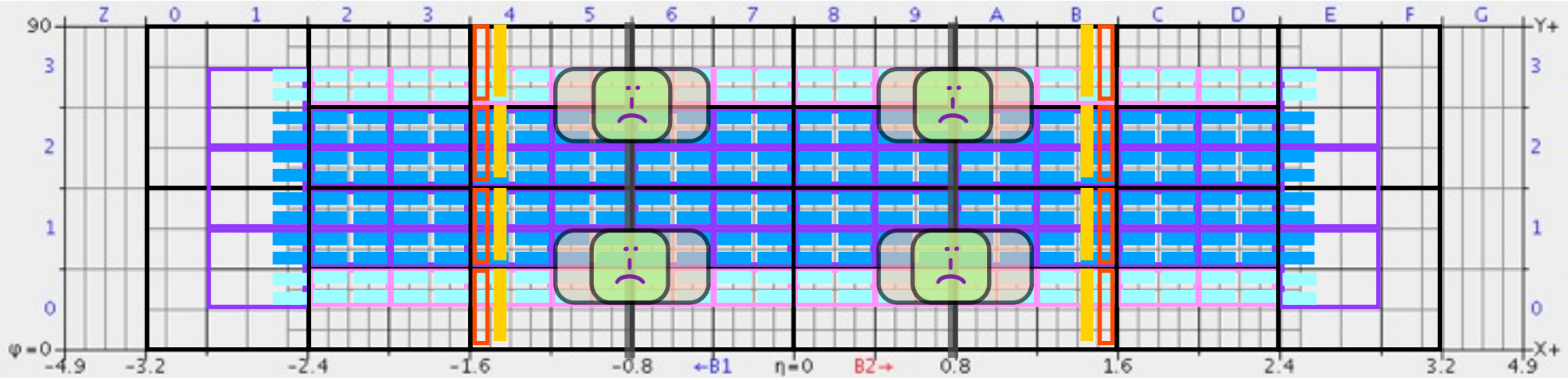


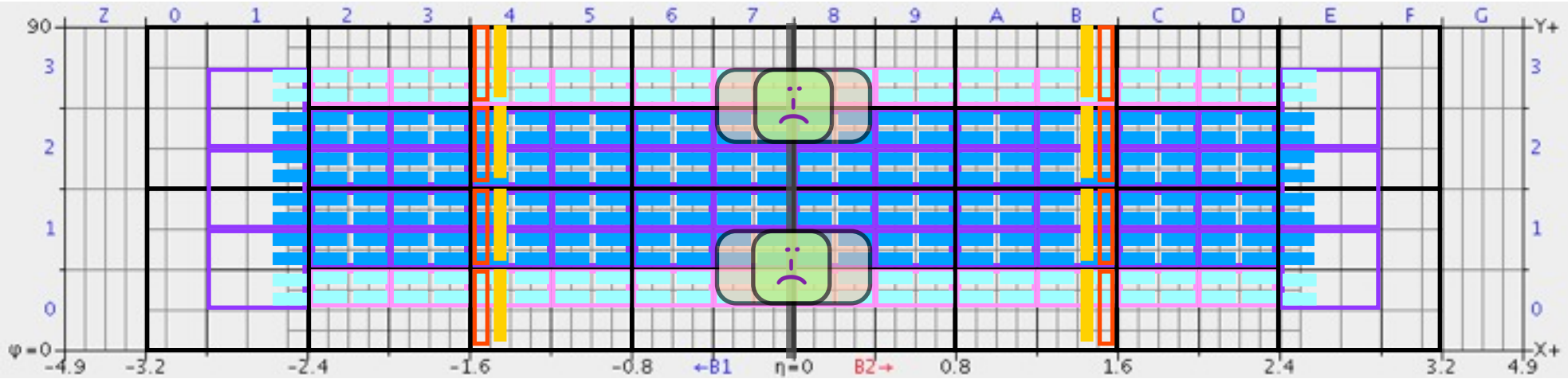
eFEX With Many Corners :-(

- Divide eFEX by both eta and phi: introducing corners
  - Split at +/- 0.8 to avoid complications at barrel/endcap
    - Core coverage roughly 1.6*0.8 => 24 modules in two crates
  - Needs quadruplication of inputs at the corners
    - Two extra supercell fibres per DPS EM mezzanine
      - Four different configurations needed => switching or firmware variants??
    - Extra Tile fibres every other 0.4 in phi at 0.4<|eta|<1.2
      - Add minipods to all phase 1 & 2 Tile sources, but only actually needed on some modules
  - For 0.5*0.5 environment: 120 EM fibres + 36 had + 8 overlap?
    - 10 or 20 fewer EM fibres for 0.4*0.4 or 0.3*0.3 environments



eFEX With Fewer Corners :-(

- Divide eFEX by both eta and phi: introducing corners
  - Split at eta=0 to avoid complications at barrel/endcap
    - Core coverage 2.5*0.8 => 16 modules in two crates
  - Needs quadruplication of inputs at the corners
    - Two extra supercell fibres per DPS EM mezzanine
      - Four different configurations needed => switching or firmware variants??
    - Extra Tile fibres every other 0.4 in phi at 0.4<|eta|<1.2
      - Add minipods to all phase 1 & 2 Tile sources, but only actually needed on some modules
  - For 0.5*0.5 environment: 168 EM fibres + 45 had + 8 overlap?
    - 14 or 28 fewer EM fibres for 0.4*0.4 or 0.3*0.3 environments



eFEX Module Fibre Counts

- Fibre count for whole eFEX module (full eta strip)

Environment	EM Fibres	Hadronic Fibres	Total Fibres	N. Ribbons
0.3*0.3	6 * 26 = 156	3 * 14 = 42	198	17 (18?)
0.4*0.4	7 * 26 = 182	4 * 14 = 56	238	20 (26?)
0.5*0.5	8 * 26 = 208	4 * 14 = 56	264	22 (26?)

- Fibre count per FGPA for four FPGAs/module

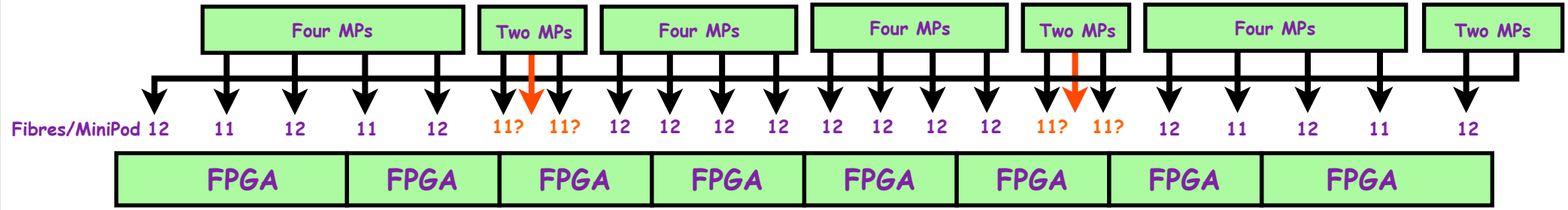
Environment	EM Fibres	Hadronic Fibres	Total Fibres	Fan In/Out
0.3*0.3	6 * 8 = 48	3 * 5 = 15	63	18
0.4*0.4	7 * 8 = 56	4 * 5 = 20	76	22
0.5*0.5	8 * 8 = 64	4 * 5 = 20	84	24

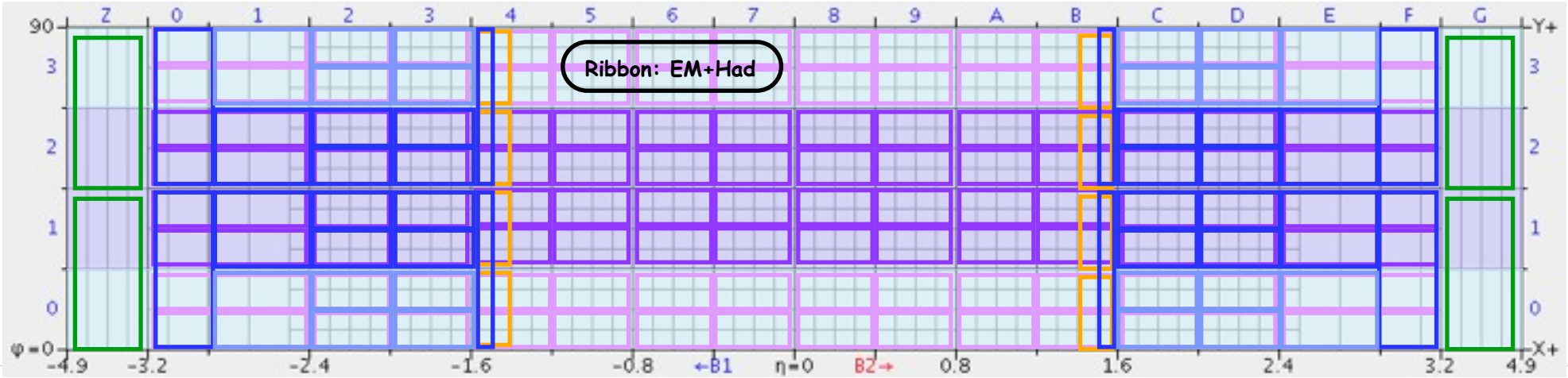
- Fibre count per FPGA for six FPGAs/module

Environment	EM Fibres	Hadronic Fibres	Total Fibres	Fan In/Out
0.3*0.3	6 * 6 = 36	3 * 4 = 12	48	18
0.4*0.4	7 * 6 = 42	4 * 4 = 16	58	22
0.5*0.5	8 * 6 = 48	4 * 4 = 16	64	24

Mapping to jFEX Module

- Orient in phi with modules handling all eta * 0.8 phi?
  - Funny business at high eta and FCAL the same for all modules
    - Roughly same fibre counts as dividing into eta stripes
      - Still expect ~256 fibres per module (22 minipods) and eight FPGAs
    - May need extra fibres at EM barrel/endcap boundary
    - To optimise FCAL ribbons, core shifted by 0.4 in phi





Uses of Spare EM DPS Fibres

- EM DPS (probably) has some spare fibres
  - Need 20 fibres (16 eFEX + 4 jFEX) for 0.8*0.4 area (1 copy)
  - 24 fibres available (48 for two copies)
- Potential uses:
  - Extra copies of some eFEX fibres to handle corners
  - Extra copies of jFEX fibres to allow for larger jets
- No spare HEC fibres?
  - Both above potential uses would need extra HEC & Tile copies

Active Patch Panel?

- Recent suggestion to have more active patch panel?
  - Provide extra copies where we need them
  - Less coupling between FEX and DPS geometries
    - Though groups of supercells/towers on single fibres still constrained
  - NB if we do this, would it provide all duplication?
    - LAr might like to reduce number of micropods per DPS mezzanine?

What If No BCMUX?

- Some people are unsure about the BCMUX scheme
  - Worry about losing signals with high pileup at 25ns operation
    - NB with 50ns operation so far, existing BCMUX not yet tested in anger?
- No BCMUX implies approximately double bandwidth
  - NB even going from 6.4 to 10 Gbit/s may not be enough
    - Unless we drop back to the 1141 scheme or use less dynamic range
  - With BCMUX we have 110 bits per two TT => one fibre @ 6.4
    - Leaving a few spare bits for extra info (quality bits), checksums etc
  - No BCMUX, have 200 bits per two TT
    - Might exactly squeeze into 10 Gbit/s, but not 9.6?
      - No room for extra info (quality bits), checksums etc

Miscellaneous Notes

- Hadronic mapping (Needs 4 copies: 2*eFEX + 2*jFEX)
  - Should be OK for Tile from PPM or JEM (0.4 or 0.8 in eta)
  - HEC from LAr DPS also OK?? (Check!) But only 2 copies?!
  - However there is a difficult boundary at |eta|=1.5
    - Need one fibre for 1.5<|eta|<2.0 to carry 10 trigger towers
      - Lower dynamic range or more aggressive non-linear encoding?
    - Or else we need an extra fibre (duplicated) for HEC 1.5<|eta|<1.6
    - Similar problem for Tile if we include crack/gap scintillators??
- Readout Checksums
  - Proposal to send checksums from DPS to FEXes
    - To avoid readout of FEX inputs - unless there are checksum errors
  - How do these fit onto the proposed fibre mapping??
- High eta region (EM)
  - Could use one EM 0.1*0.2 fibre for 2.4<|eta|<2.5
    - Or else keep two 0.2*0.1 fibres and send the high eta region just in case?

Summary

- L1Calo "hoped for" mapping sketched
- Still needs a lot of detailed work…
  - Discussion with LAr experts
    - NB they are currently working to the 0.4*0.2 shape DPS mezzanine FPGA
  - Documentation, documentation
  - All to be done soon to allow eFEX & jFEX specification

Spare: Grids for Doodling