gFEX Functionality via jFEX?

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- Introduction
- Pileup calculations
- Fatter jets (in phi and eta)
- Phi ring jFEX
- Summary and questions

Introduction

- Play devils advocate and try to avoid gFEX hardware
  - Can requested gFEX functionality be provided by jFEX?
  - And can jFEX do better than the TDR gFEX??

- NO - if we must stick to TDR baseline 6.4 Gbit/s links
- But lets assume 10 Gbit/s links (ideally 11.2)

- Two requested gFEX functions (as far as I know)
  - Calculating estimate of event by event pileup
    - This then needs to be subtracted from jets and missing Et
  - Increasing the jet window
    - Way beyond TDR baseline jFEX window of 0.9*0.9
    - Ideally also beyond 1.7*1.7 suggested for 10 Gbit/s jFEX

Calculating Pileup

- gFEX request is really to do this in phi rings
  - Required granularity in eta is not clear - full eta range needed
- Can this be done with jFEX oriented in eta strips?
  - One jFEX module covers all eta by 0.8 in phi
    - All jFEX modules have a small equal dose of barrel/endcap/FCAL issues
- jFEX at 10 Gbit/s: 0.8 phi core + 2 * 0.8 environment
  - So each jFEX sees 24 of the total 64 phi bins
  - My original idea was to estimate pileup median from 24 towers
    - Then send 8 median estimates (per eta range) to L1Topo
  - How many fibres can we use for this...? [PTO]
    - Assuming 1 fibre at 11.2 Gbit/s => 216 bits (+8 bit CRC)
    - Say 8 bits per pileup median => 27 possible values
  - Eta range is 82 (50 central, 8 forward, 2*12 FCAL1)
  - So roughly one pileup median per 3 eta bins

Phase 1 L1Topo Inputs

- Updated proposal following L1Calo meeting
- L1Topo FPGA1:
  - 48 eFEX EM fibres (2/eFEX module)
  - 24 jFEX jet fibres (3/jFEX module)
  - 4 muon fibres (NB copied to both FPGAs)
  - 4 spare fibres
- L1Topo FPGA2:
  - 48 eFEX Tau fibres (2/eFEX module)
  - 8 jFEX energy sum fibres (1/jFEX module)
    - Here I assumed a couple of Ex/Ey and Et sums
  - 4 muon fibres (NB copied to both FPGAs)
  - 20 spare fibres
- So we could use 1 or 2 fibres/jFEX module for pileup
  - Using two leaves almost no spare inputs for future ideas...

What David Actually Wants...

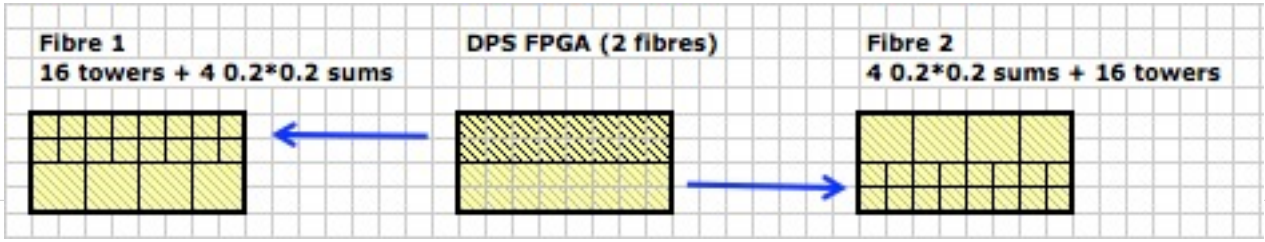
- However my proposal is not what is really wanted!
- Instead David suggests several values per eta range
  - Et vector of all towers: 12 value + 3 bit direction (local phi)
  - Vector of towers with Et below a cut Ethresh (7+3 bits)
  - Sum Et of towers below the cut (7 bits) => pileup estimator
  - Total 32 bits per eta range
- Send this on either 2 or 3 fibres
  - This is my pair of energy and pileup fibres (plus one more?)
  - At 11.2 Gbit/s, two (three) fibres allows 432 (648) bits
  - That allows 13 (20) eta ranges
    - Probably 20 is OK, 13 too few?
  - And uses a lot of L1Topo inputs
- Later on will consider jFEX in phi rings

Fat Jets: Introduction

- 10 Gbit/s jFEX offers 1.7*1.7 jets sliding by 0.1
  - There is 0.8 eta and phi environment around each core tower
- But TDR gFEX suggests sliding by 0.2
  - And only offers a slightly larger window of 1.8*1.8
- But jFEX with 0.2 sliding windows offers the same!
  - 2*0.8 environment around each tower + core 0.2
  - And gaussian weighting calculations can still be done at 0.1
  - [Reminder: only if we are allowed to assume 10 Gbit/s links]
- Is there any chance of even fatter jets?
  - Consider schemes for wider in phi or eta or both
    - Only sliding by 0.2 (surely no bandwidth for 0.1)
    - NB not much thought so far => could be overlooked killer problems
  - Following diagrams are for eta oriented jFEX modules
    - Similar options possible for phi ring jFEX modules (with eta <-> phi)

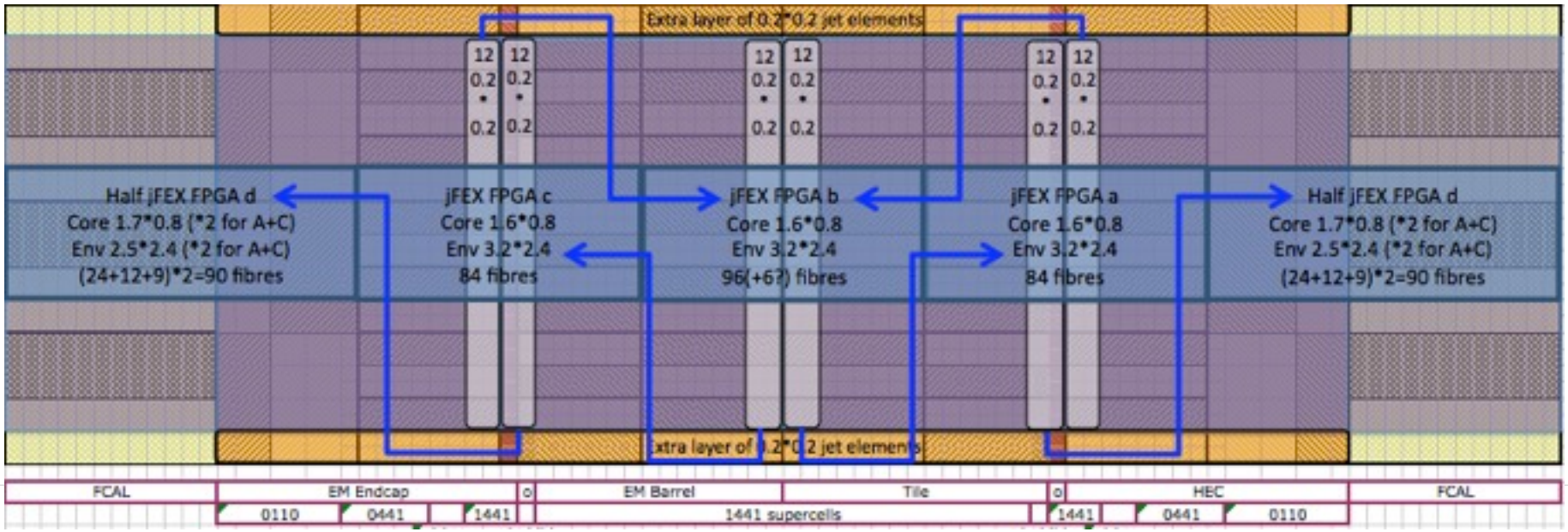
Fatter in Phi

- LAr DPS FPGAs cover 0.8*0.4 in eta*phi (central EM)
  - Proposal at 10 Gbit/s: two fibres each covering 0.8*0.2
  - Sixteen 0.1*0.1 towers per link
    - 11 (13) bits/tower available at 9.6 (11.2): 13 ample, 11 still OK?
    - Originally some ideas of special Ex/Ey/E sums per FPGA (top slice bits)
      - But probably this ideas is not useful given David Stroms recent input
- Suggestion:
  - Squeeze n.bits/tower and add four 0.2*0.2 sums from the other half of each FPGA (probably only at 11.2 Gbit/s)
    - 16 * 11 bits/tower + 4 * 10 bits/sum = 216 bits + 8 bit CRC = 224 bits
  - Shift core jFEX coverage by 0.2 to span centre of DPS FPGAs
  - Can have 1.8*2.2 (eta*phi) jets sliding by 0.2

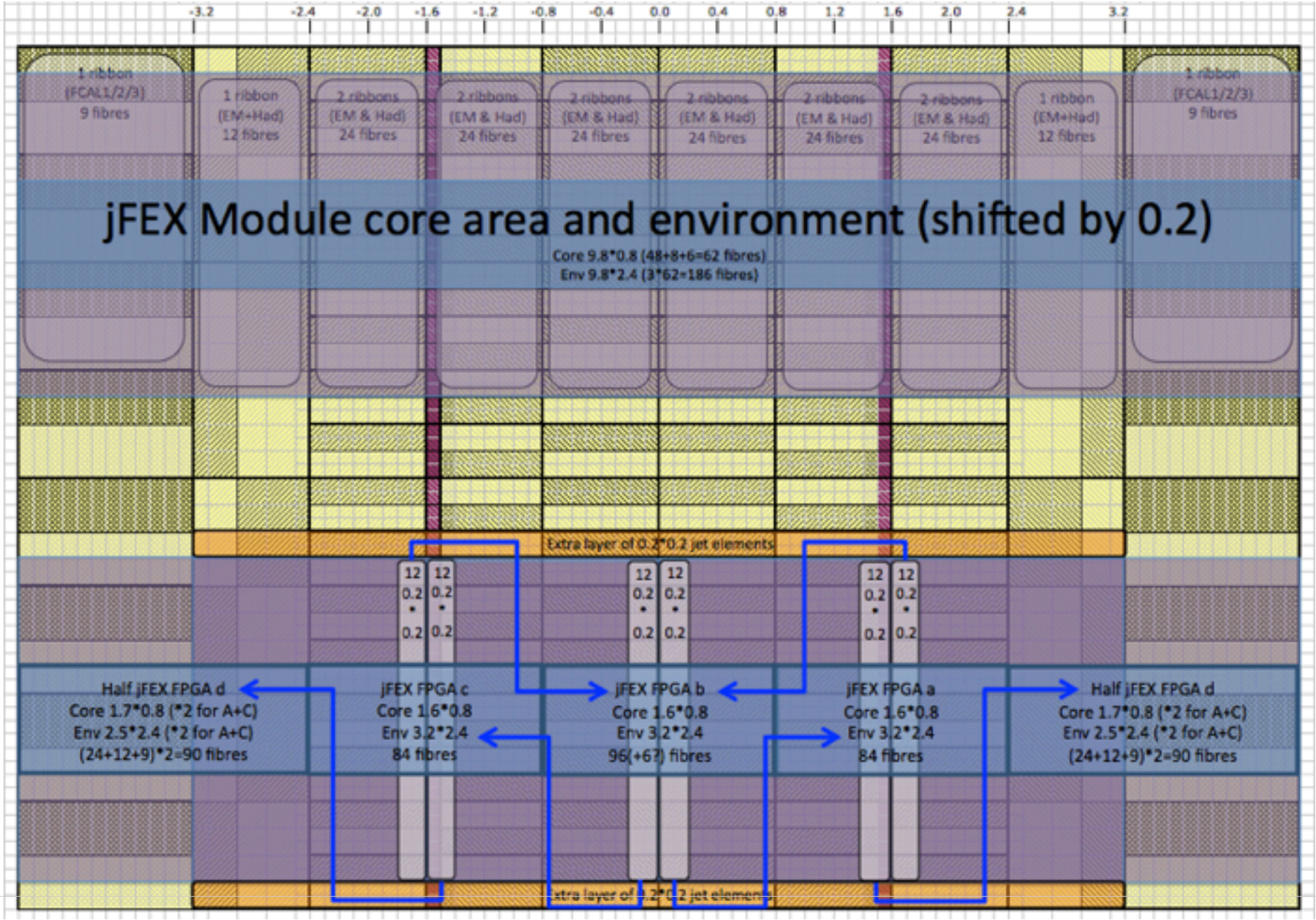


Fatter in Eta

- jFEX FPGAs are full of high speed input fibers
  - Suggestion: what about low speed (1 Gbit/s) links?
  - Consider sending slice of 12 0.2*0.2 sums to neighbour FPGA
    - Actually 24 sums if we keep EM and hadronic separate (if needed??)
  - One 1 Gbit/s link sends 25 bits/BC => two 0.2*0.2 sums
    - Need 6 (or 12) links per slice for EM+Had (or separate EM and Had)
      - Six such slices on the PCB => 36 (or 72) links in total - is that too many??
    - If its OK, could have 2.2*1.8 (eta*phi) jets sliding by 0.2



Overview Diagram



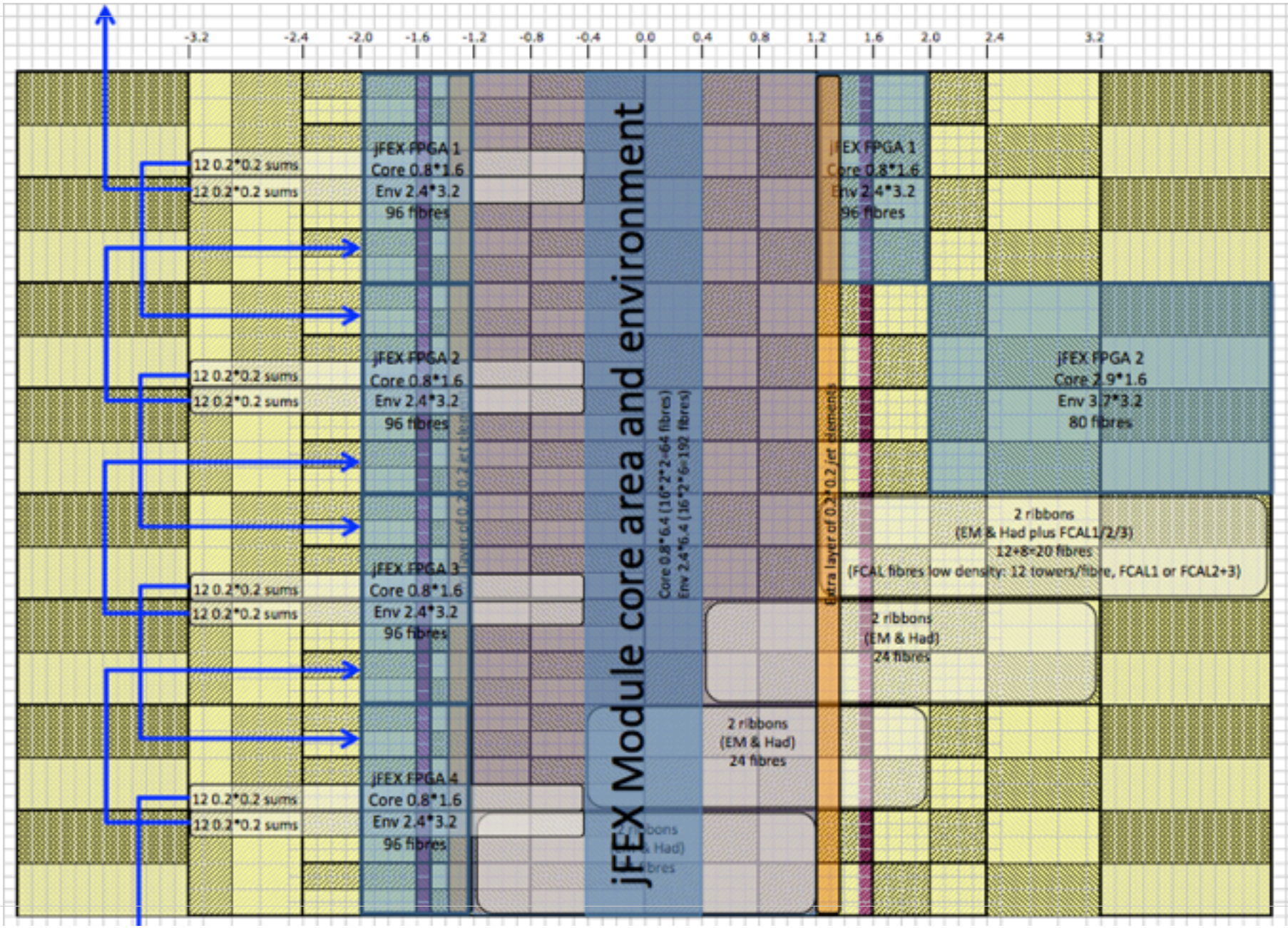
Fatter in Eta and Phi

- Could use both options together (if both are viable)
  - That might allow 2.2*2.2 jets sliding by 0.2
    - NB this implies a few extra 1 Gbit/s links for extra phi coverage
- Caveats and questions
  - Is it actually useful to have fatter jets in one direction only?
  - Adding jet element sums to fibres limits n.bits/tower
    - Not really sure how many bits/tower we really need
      - At least it seems there may not be a need for Ex/Ey/E sums from the DPS
  - Adding tracks to jFEX PCB increases complexity
    - NB in the four 96-input FPGA design, a few 1 Gbit/s links would also be needed for replicating the HEC overlap towers for one eta position
      - Though quite possibly no one would notice a small inefficiency
    - Retransmission over these links has a ~1 BC latency penalty
  - Shifting jFEX core by 0.2 is clearly ugly for FCAL
    - Probably OK for HEC and forward EMEC but not studied in detail

Phi Ring jFEX Modules

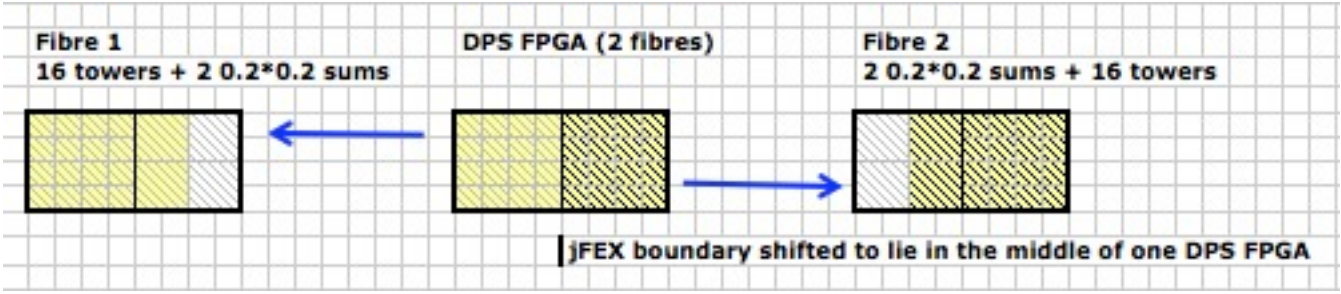
- NB not mentioned in my megamail
- Pileup corrections much easier with phi ring jFEX
  - No need for additional L1Topo fibres
- Look at phi ring jFEX architecture
  - Mainz has already done this I think
  - And still try to allow for fatter eta/phi jet options
    - Needs jFEX core shifted by 0.4 in eta
      - Central jFEX module spans eta=0
      - Only need seven modules (cf eight in eta oriented scheme) => fewer L1Topo inputs
- BUT (or maybe just but)
  - No space for HEC overlap fibres (as environment)
    - Some corresponding loss of efficiency
      - But this only affects outlying part of jet so perhaps not too bad?
  - Need more 1 Gbit/s links for fatter phi option
  - Fatter eta option needs different fibre geometry => Tile?!

Phi Ring jFEX Diagram



Phi Ring Fibres and Tile Inputs

- Fatter eta option => fibre covers 0.4*0.4
  - Only need 2 extra 0.2*0.2 sums => may even work at 9.6 Gb/s
    - Have 10 bits/tower (or sum) at 9.6, comfortable 11 bits/tower at 11.2
  - OK for LAr EM, probably OK for HEC and EMEC forward
    - Need to check impact on eFEX: maybe shift eFEX core by 0.2 in phi?

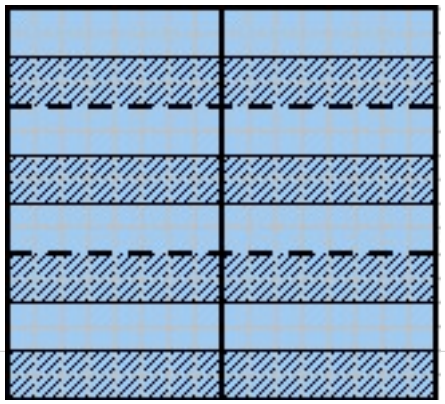


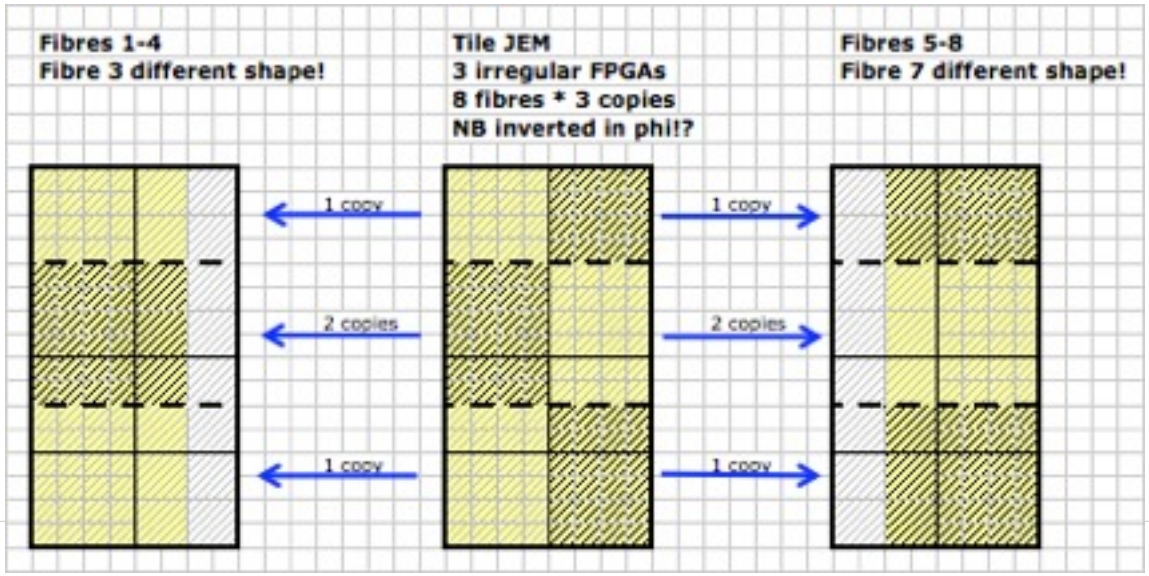
  - Would need to insist Tile phase 2 electronics covers 0.4 in phi
  - What about Tile input at phase 1?

Phi Ring Tile Input at Phase 1

- Division of JEM towers into FPGAs is awkward!
  - But can be made to match neatly for eta oriented jFEX
  - 0.8*0.2 fibres also match Tile preference for phase 2
- Ugly solution is possible with 0.4*0.4 shape fibres
  - Assuming at phase 1 we still only have 8 bits/tower
  - Can fit 24 towers per 11.2 Gbit/s fibre (but not 9.6!)
    - And at 11.2 also have room for 2 or 3 0.2*0.2 sums
      - 27*8 bits = 216 + 8 bit CRC = 224 bits exactly

2*JEM fibres to eta oriented jFEX (wrong way up in phi)





Summary

- My personal opinion:
  - gFEX functionality can be done in 11.2 Gbit/s jFEX
    - And jFEX might be able to provide even fatter jets than TDR gFEX
- But nothing comes for free!
  - Price includes one or more of: fewer bits/tower, ugly match to FCAL, loss of efficiency for HEC overlap in some places, extra complexity of jFEX PCB, 0.4 phi modularity in Tile at phase 2, etc
- And uncertain link speed means we cannot choose now

(Initial) List of Questions (1)

- Pileup related (eta oriented jFEX)
  - Is median of each jFEX median a good enough estimator?
  - Are Davids bit counts adequate?
  - Is the possible number of eta ranges enough?
  - Is this taking up too many L1Topo inputs?
- Fatter jets (>1.8 in eta or phi or both)
  - N.bits/tower required? Also n.bits/sum (jet element)?
  - Is there really no need for Ex/Ey/E from DPS?
  - Is it helpful if jets can only be fatter in one direction?
  - Are there problems with FCAL in jFEX shifted by 0.2 in phi?
  - Can we use additional 1 Gbit/s links on jFEX PCB?
  - Is a 1 BC latency penalty (a) possible (b) a worthwhile price?
  - How sensitive are such huge jets to hardware problems??

(Initial) List of Questions (2)

- Political
  - Can the MoU be written to require gFEX functionality but allow implementation by jFEX if link speeds allow?