FEX Outputs to L1Topo

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(with help from Jim
and L1Topo experts)
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- Suggestion for FEX links to L1Topo
- Open questions

Background: eFEX design

- How many fibres should eFEX send to L1Topo?
  - Would like to know for eFEX design (PDR)
- While we are at it, how many from jFEX, muons, etc?
- Constraints:
  - L1Topo has 160 input fibres (80 into each of two FPGAs)
  - There are 24 eFEX modules and 8 jFEX modules
    - Large number of eFEX modules => few fibres per module
  - Algorithms may want all EM, Tau, Jet, Muons in one FPGA
  - Limited possibility to share data between FPGAs
    - 238 links of up to 1 Gbit/s: fairly small fraction of input bandwidth

Input Data

- Need to define phase 1 TOB data formats
  - Some suggestions in last L1Calo Thursday meeting
    - https://indico.cern.ch/conferenceDisplay.py?confId=276099
- EM/Tau
  - Probably 30 bits, 4-7 TOBs/fibre (depends on link speed)
  - Are EM and Tau separate TOBs? Or are overlaps removed?
- Jet
  - No detail yet: TOB probably larger than EM/Tau?
- Energy
  - Only few values, special format
- Muon
  - Similar to EM/Tau?
  - Already merged by new MuCTPI (presumably?)
    - TDR suggests one fibre per quadrant => 4 fibres total

Fibre Counts from Jim...

- Spreadsheet with phase 0 details and phase 1 ideas

	inputs				non zer su	act			L1topo:						
			design	fiber	NoOsuppre	actual	fiber			Topo inputs:					
Run	type	modules	tob/mod	bit/tob	fib/mod	fib/mod	speed	bits/fibe	tob/fibe	fibers	tobs				
2	*CPM*	*48*	*5*	*25.5*	*1.00*	*0.5*	*6.4*	*128*	*5.02*	*24*	*120*	*cmx does zero suppress*			
3	efex	24	10	32	2.50	3	6.4	128	4	72	288	same tob density as Run 2		avoid	
3	efex	24	12	32	2.00	2	9.6	192	6	48	288			sweet spot	
3	efex	24	14	32	2.00	2	11.2	224	7	48	336			headroom, but not fewer fibers	
2	*JEM*	*32*	*4*	*32*	*1.00*	*0.5*	*6.4*	*128*	*4.00*	*16*	*64*	*cmx does zero suppress*			
3	jfex	8	16	40	5.00	5	6.4	128	3.20	40	120	same tob density as Run 2			
3	jfex	8	10	40	3.13	4	6.4	128	3.20	32	96	jfex does zero supp		too much zero suppression?	
3	jfex	8	14	40	2.92	3	9.6	192	4.80	24	96	jfex does zero supp		sweet spot?	
3	jfex	8	16	40	2.86	3	11.2	224	5.60	24	120	jfex does zero supp		headroom, or perhaps fewer fibers	

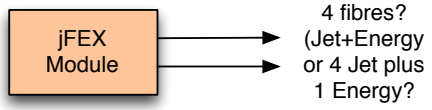
topo fiber usage		(2 fpga/board)				fiber	fpga in						
	fiber/fpga		fpga xfer GB/s			speed	GB/s	% xfer max					
	80		238			6.4	512	46%					
	80		238			9.6	768	31%					
	80		238			11.2	896	27%					

	em	tau	j	E	mu	total fibers (one copy of inputs)		
Run 2 fibers:	24	24	16	4	2	70		2 copies/board
Run 3 fibers:	48	48	24	4	4	128		only 1 copy/board
R3 worst case	72	72	40	4	16	204		< 1 copy/board

Strawman Suggestion (1)

- Keep EM and Tau as separate TOBs
  - Two EM plus two Tau fibres per eFEX (to each L1Topo)
    - Total 48 EM + 48 Tau fibres to each L1Topo

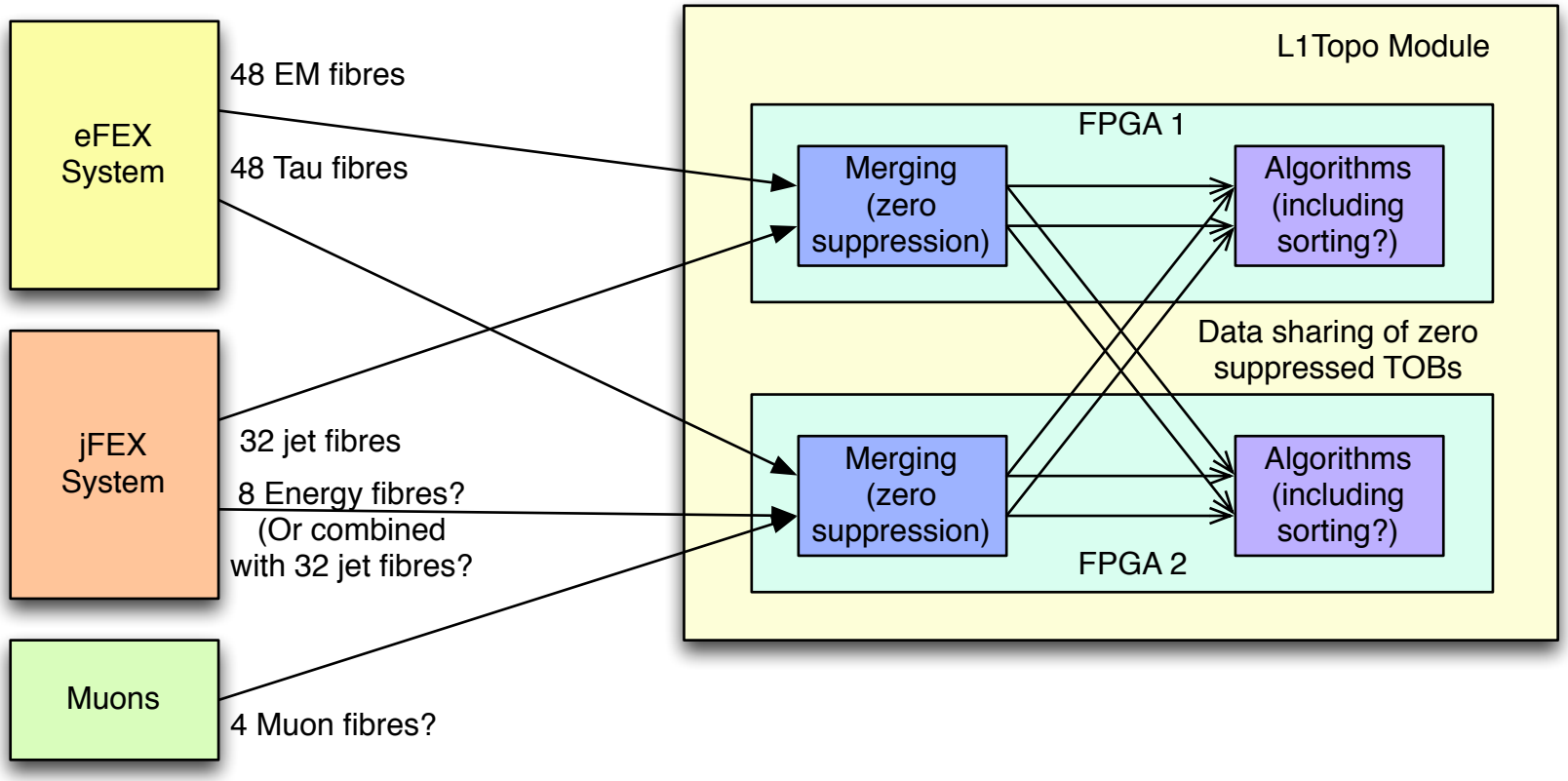
- 3 or 4 fibres per jFEX module to each L1Topo
  - 24 or 32 fibres total (jets only?)
    - Maybe Energy "TOBs" on separate jFEX fibre?
    - And yet one extra fibre for 0.4 granularity pileup sums???



- Four muon fibres total
- One copy per L1Topo (NOT one copy per FPGA)
- Assume maximum data sharing between FPGAs
  - Must be done after input data merged (zero TOBs removed)
  - O(100) links in each direction sending 25 bits/BC
    - Assume two links needed per TOB => about 50 links each way
  - Can share 25 EM + 25 Tau + 25 Jets + 25 Muons + Et sums
    - Also need to send overflow flags for each category
- Possible to have all useful data in both FPGAs

Strawman Suggestion (2)

- Data sharing:
  - EM+Jets sent from FPGA 1 to FPGA 2
  - Tau+Muons(+Energy?+Pileup?) sent from FPGA2 to FPGA 1



Questions

- Is this proposal basically viable?
- Open questions
  - Described links to one L1Topo
    - Need copies for each L1Topo - how many of them??
    - Assume 4 L1Topos => 16 output fibres per eFEX
    - But make provision (how much?) for more output fibres at phase 2
  - Separate EM and Tau TOBs (or single merged EM+Tau)?
    - Latter implies different model for sharing between FPGAs but still OK
  - Separate Jet and Energy TOBs from jFEX?
  - Is the bandwidth limit on the number of TOBs per eFEX or jFEX acceptable? Needs further simulation...
  - Bottleneck likely to be the interFPGA data sharing on L1Topo
    - May need more compression here?
  - Detailed work on TOB formats still required