L1Calo: Common Infrastructure
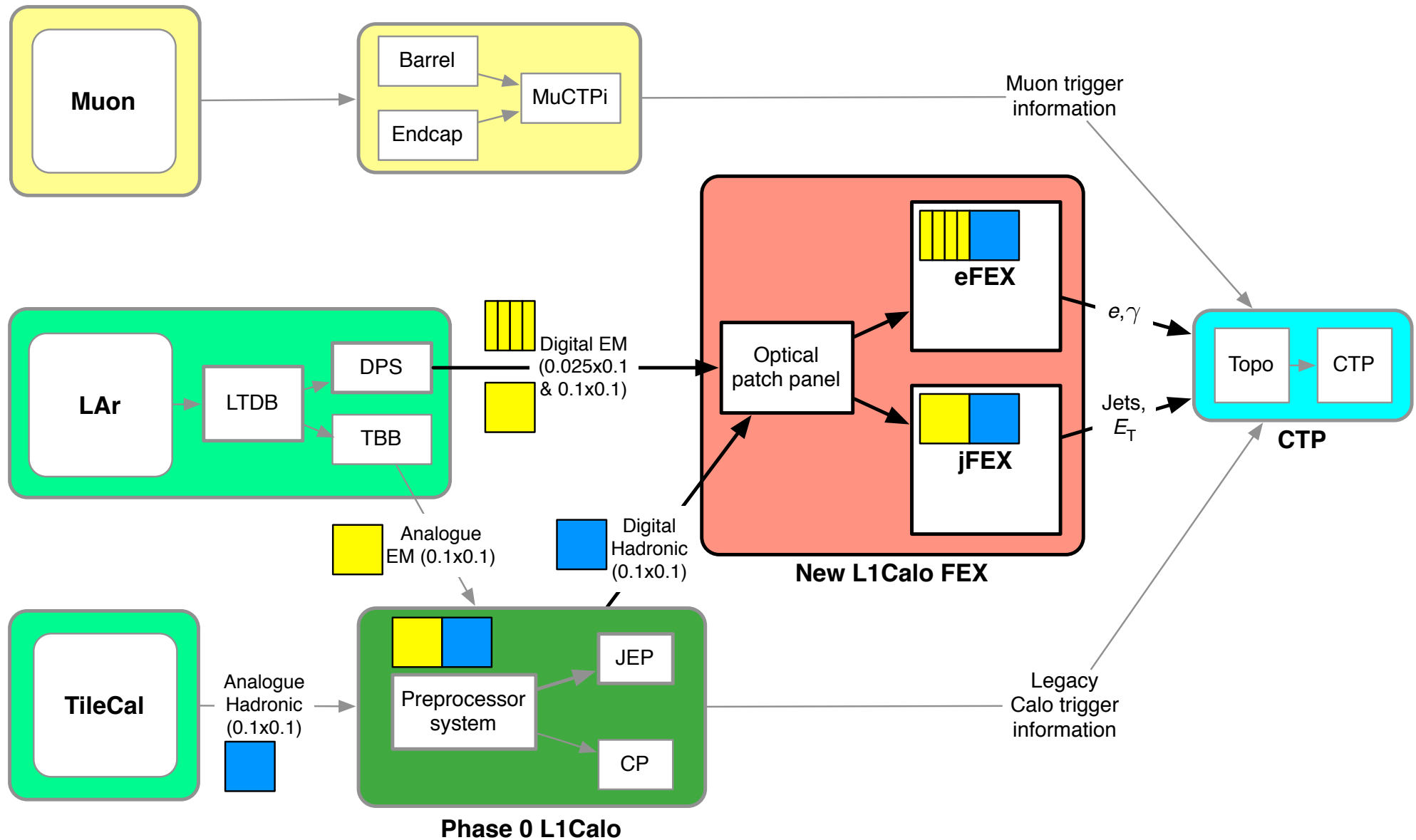## (Reprise of talk at TDAQ IDR)

Murrough Landon
13 March 2013

- Overview
- Optical Patch Panel
- Common ROD Daughter Card
- ATCA Hub Module (TTC/Busy/Control)
- IPMC Interface (DCS)
- ATCA Crate Installation
- Firmware and Software
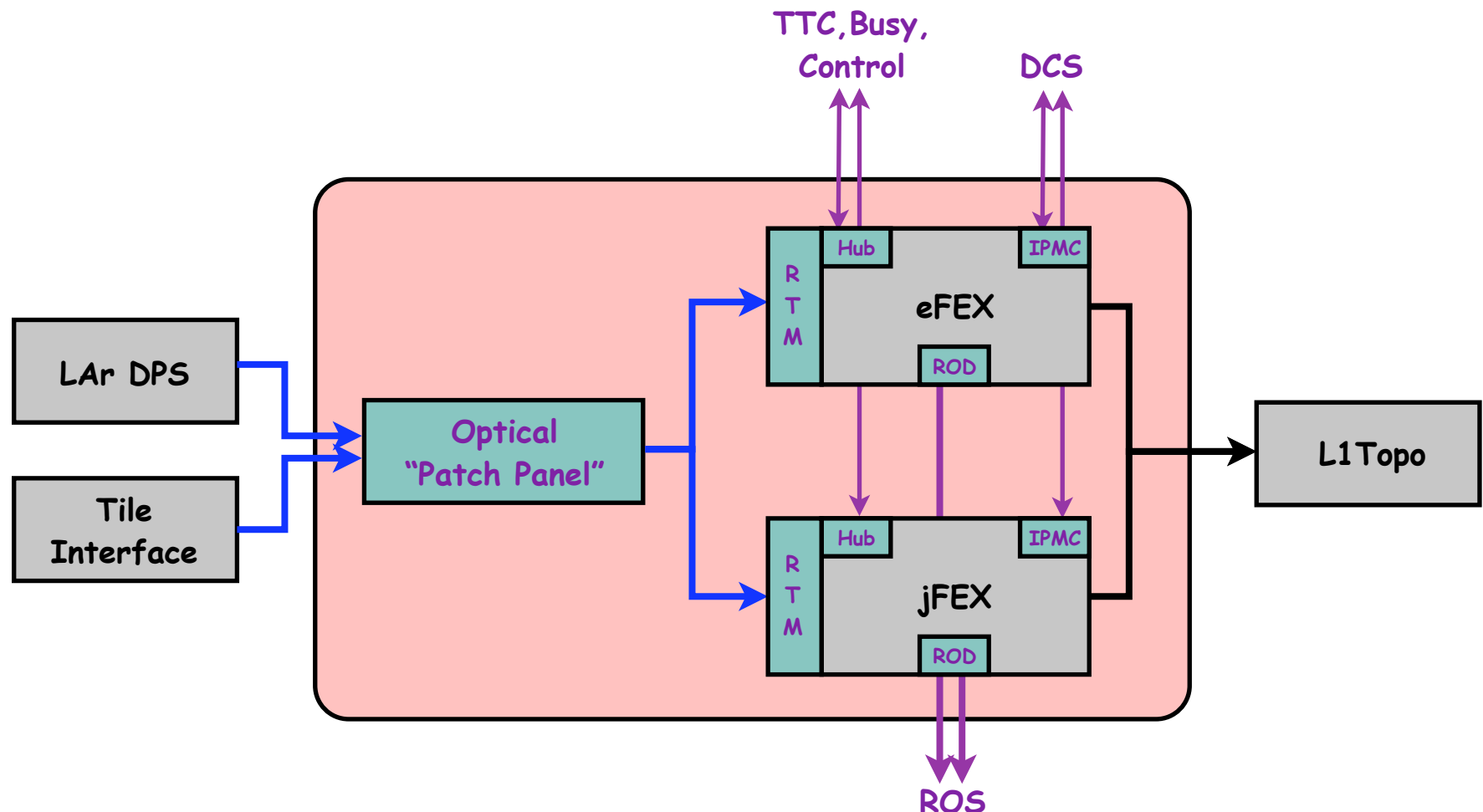- Schedule for Common Items
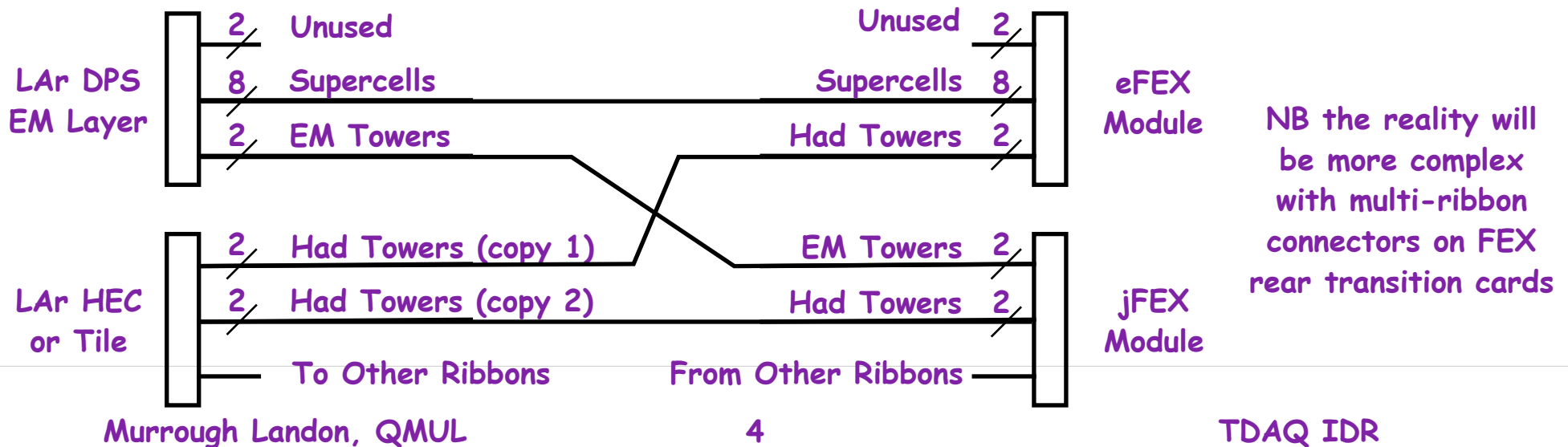- L1Calo Work Packages

Overview

Overview

- Common infrastructure for eFEX and jFEX
  - All the colourful parts of this diagram...

Optical Patch Panel

- Interface between LAr DPS or Tile and the FEXes
  - Mapping onto regular eta phi space for sliding windows
    - Regrouping fibres into ribbons destined for eFEX vs jFEX
      - Eg fine granularity EM supercells for eFEX, 0.1*0.1 EM towers for jFEX
  - Additional passive optical splitting where needed
    - LAr DPS and Tile interface mostly provide enough copies of signals
    - But (probably) the HEC needs additional duplication
      - We need two copies to adjacent eFEX modules plus two copies to adjacent jFEX modules
  - Implementation as sets of "octopus" fibre ribbons
    - Needs very detailed design of the mappings, then just buy them...

LAr DPS EM Layer

2 Unused   Unused 2

8 Supercells   Supercells 8   eFEX Module

2 EM Towers   Had Towers 2

LAr HEC or Tile

2 Had Towers (copy 1)   EM Towers 2

2 Had Towers (copy 2)   Had Towers 2   jFEX Module

To Other Ribbons   From Other Ribbons

NB the reality will be more complex with multi-ribbon connectors on FEX rear transition cards

Rear Transition Module

- Brings bundles of optical fibres to ATCA Zone3
  - Rear transition module just a passive mechanical support
  - Fibres grouped into multiway optical connectors (72 fibres)
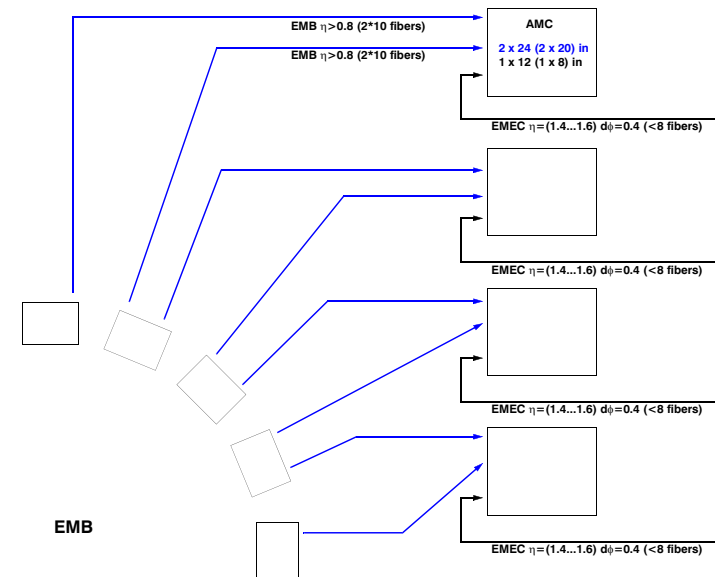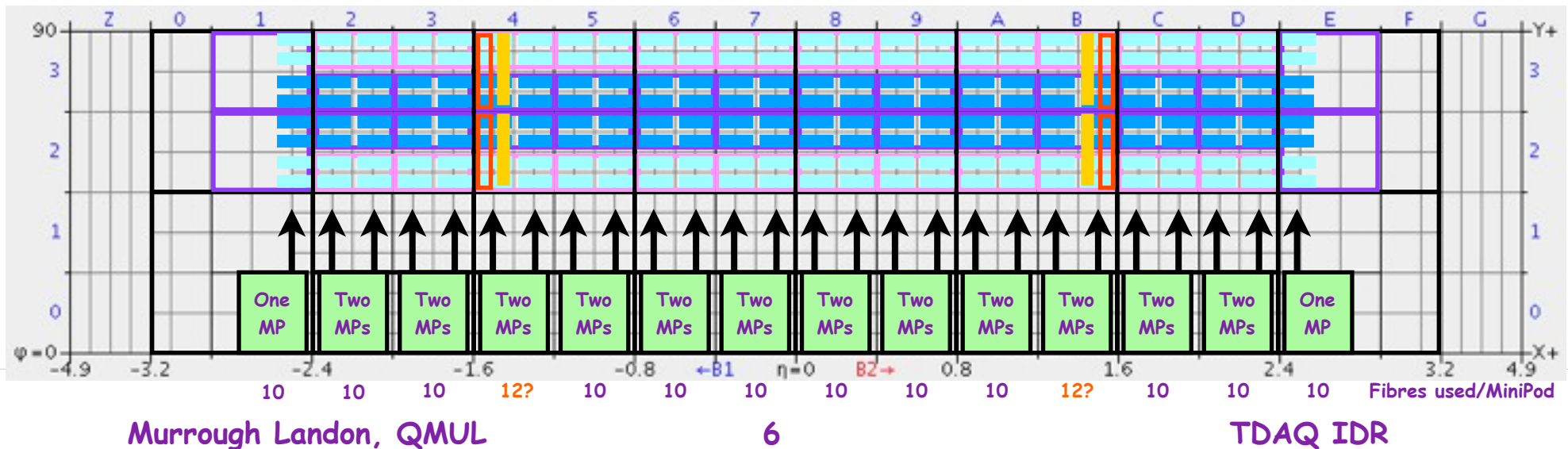 - eFEX/jFEX modules will have four such connectors
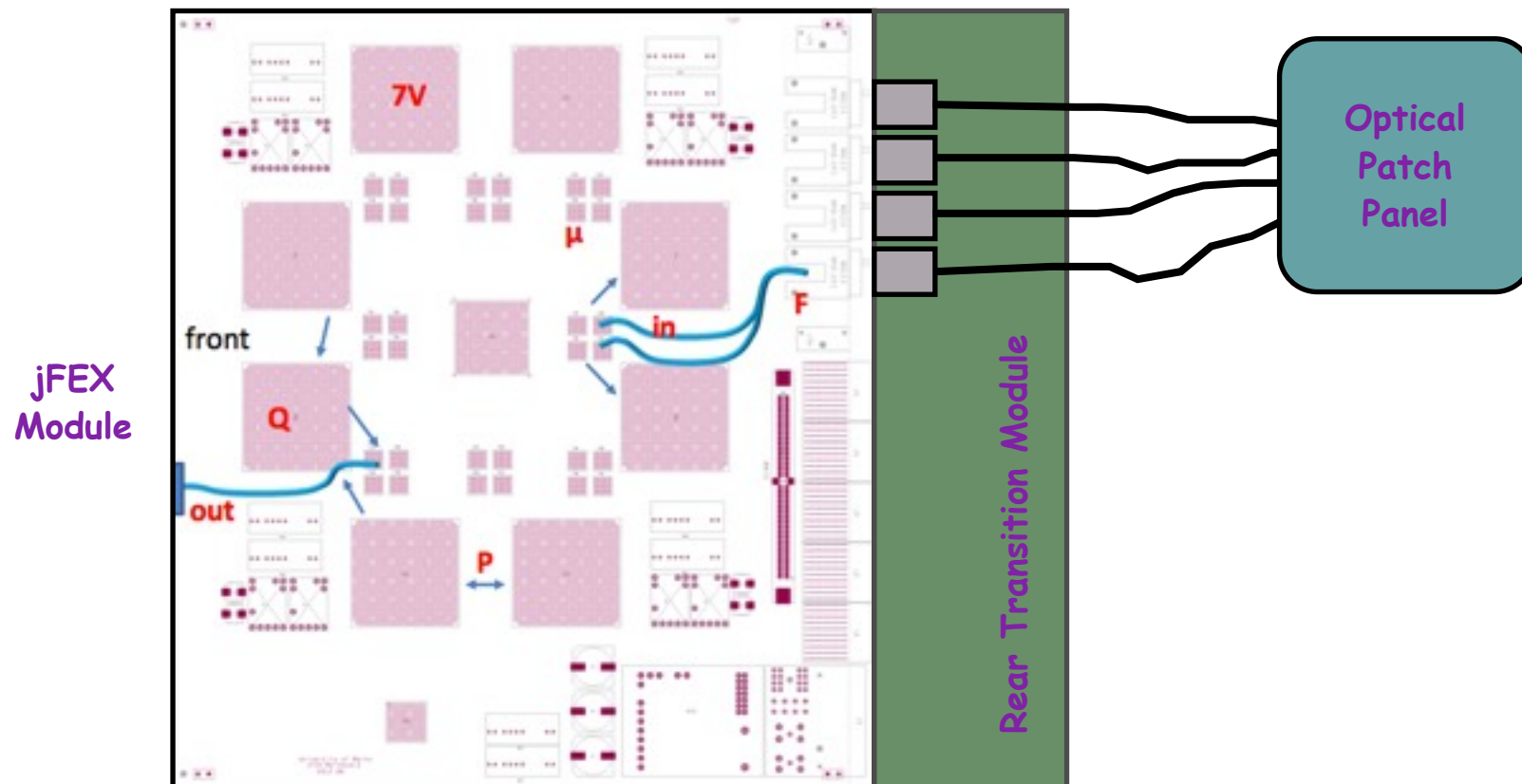
DPS/Tile to FEX Mapping

- Detailed mapping to FEXes needs to be defined
  - Sliding window algorithms need regular eta phi grid
    - May need special handling of some areas eg barrel/endcap boundary
  - Discussions started with LAr
    - Many details to be sorted out...
    - ...also with FEX engineers

Sketch for possible handling of EM barrel/endcap overlap (S.Simion)

EMB η>0.8 (2*10 fibers)
EMB η>0.8 (2*10 fibers)

AMC
2 x 24 (2 x 20) in
1 x 12 (1 x 8) in

EMEC η=(1.4...1.6) dφ=0.4 (<8 fibers)
EMEC η=(1.4...1.6) dφ=0.4 (<8 fibers)
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EMB

Design study for "worst case" mapping to eFEX module (0.5*0.5 environment)

| One MP	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	Two MPs	One MP
	10	10	12?	10	10	10	10	10	10	12?	10	10	10

Fibres used/MiniPod

ROD Daughter Card

- ## Interface to DAQ
  - Each eFEX and jFEX module acts as its own ROD
    - Needed for phase 1, must be compatible/upgradeable for phase 2
  - Implement ROD functionality as a daughter card
    - Common hardware for eFEX and jFEX, but different firmware needed
  - Emulate current Slink protocol for phase 1
  - Can change protocol for phase 2 or replace daughter card
    - But must make sure all the necessary phase 2 signals are tracked to it!
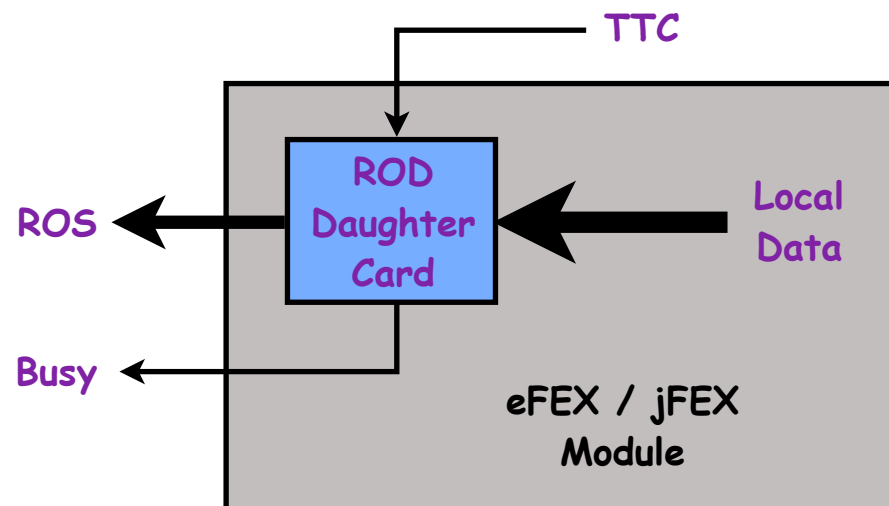
Content of Readout to DAQ

- L1Calo FEXes (and LAr DPS) are DAQ subdetectors
  - Essential to read out enough to verify operation of the trigger
  - Traditional L1Calo model: readout all inputs and outputs
    - Some duplication: output of PPM is input to CPM etc
    - But data volume reduces dramatically with each pipeline step
  - We will certainly read out the outputs of FEX algorithms
  - But replicating DPS output is a lot of data
    - So we are thinking about sending checksums from DPS to FEXes
    - Then only readout FEX input from DPS if checksums are wrong
      - Up to some bandwidth limit
  - NB this assumes the LAr DPS data is read out to DAQ
    - DPS readout is still being discussed (even one copy is quite a lot)
  - L1Calo view is that:
    - BCID result for each supercell is mandatory for every event
    - ADC samples desirable every event (mandatory on day 1, reduce later?)

ATCA Crates

- Both eFEX and jFEX will be implemented in ATCA
- We will follow the evolving ATLAS ATCA standards
  - ATLAS ATCA recommendations drafted - not yet final?
  - In some cases multiple options are suggested
- We expect to have:
  - 14 slot crates, vertical air flow, two crates per rack
  - LAPP IPMC daughter card
  - Hub module function for ethernet, TTC, busy
  - Module configuration and control via IPbus (Ethernet/IP)
    - Firmware and software package developed by CMS
      - Interest in this also from other ATLAS subdetectors (LAr) and LHCb

ATCA Control Hub

- ATCA crates need one (or two) hub modules
  - Several undemanding functions
  - Implement in low end FPGA, possibly on a daughter card
    - Capability present on all eFEX/jFEX modules but only used in hub slots
    - Some functions could be tested on UK High Speed Demonstrator
- Ethernet switch
  - Route ethernet to other modules in the crate
    - For high level module control (eg configuring the trigger) via IPbus
- TTC hub
  - One module per crate acts as TTC hub
    - TTC signals sent over ATCA zone 2 backplane
  - Alternative possibility: TTC fibre to each module
- Busy aggregator
  - Collect BUSY signals from ROD daughter cards in the crate

IPMC (DCS Interface)

- ATCA crates need low level IPMC interface
  - Low level module control, ie switching on and off
  - Collect voltage/temperature information via I2C buses
  - This should be the interface to DCS
- LAPP have produced a suitable daughter card for this
  - Very low profile miniDIMM - minimal space impact on board
  - Being recommended as the ATLAS standard
  - Available in the summer

Rack Space in USA15

- L1Calo and LAr need 3 or 4 racks in USA15
  - Should be OK: but need to (re)move less critical equipment

LAr DPS   L1Calo FEXes

LDPS1	LDPS3	Spare/Optics	eFEX1
LDPS2	Spare/Optics	jFEX	eFEX2
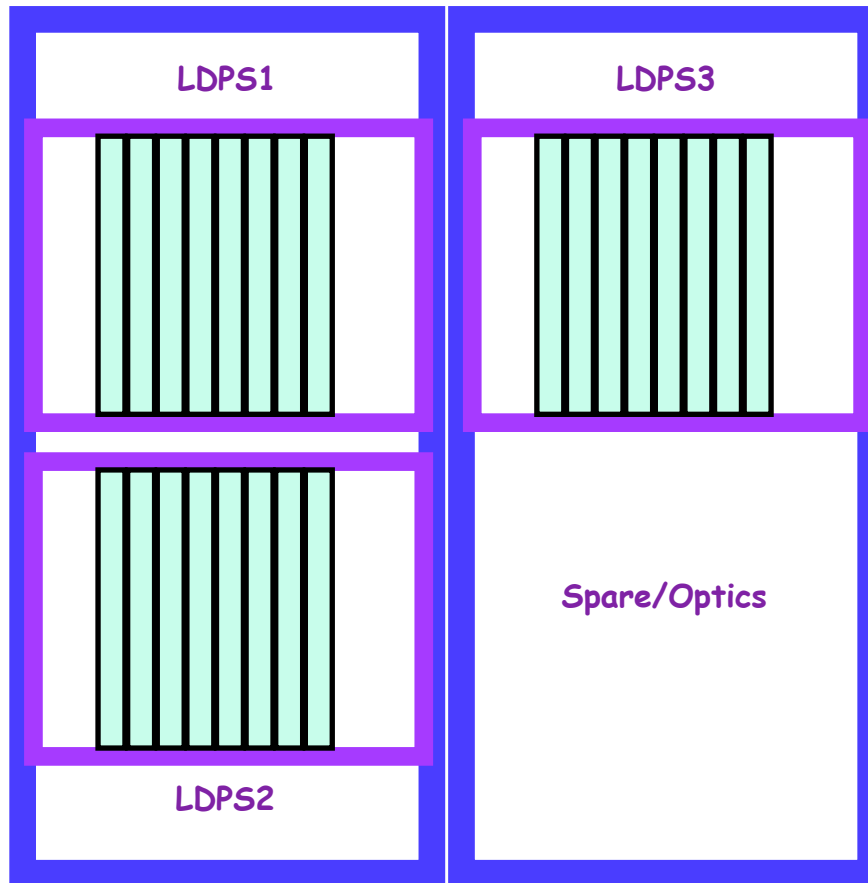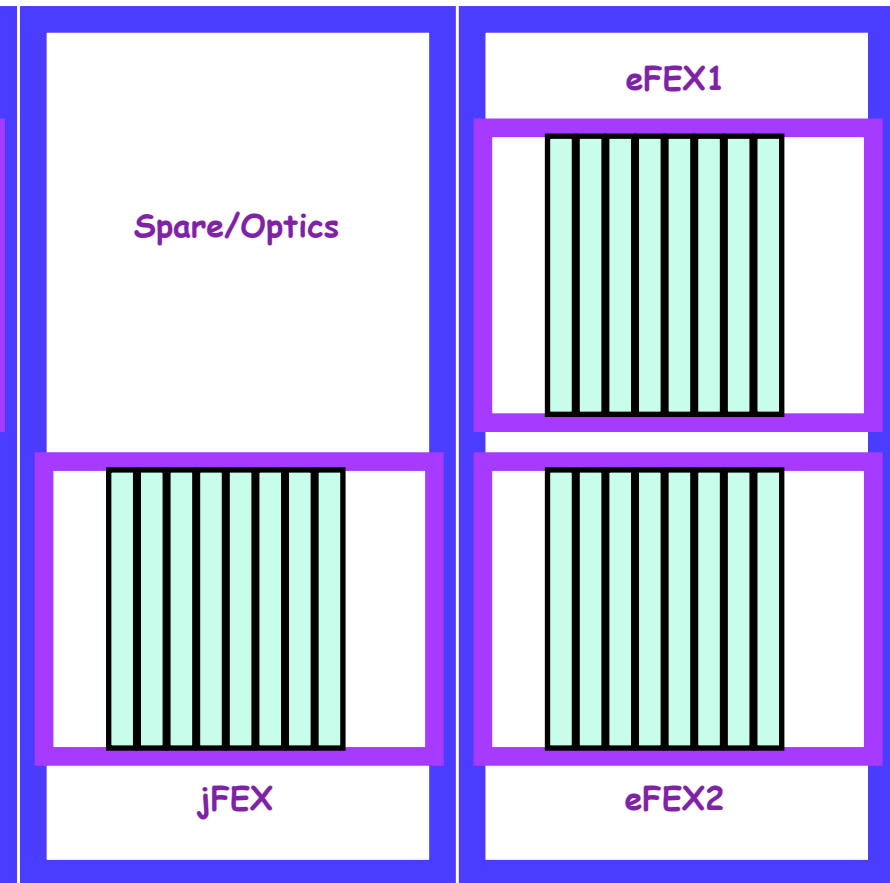
DCS/Monitoring => Move   Tile Cosmics => Remove   Empty Rack   Receiver Control => Move/Remove?

Y.29-02.A2   Y.28-02.A2   Y.27-02.A2   Y.26-02.A2

Murrough Landon, QMUL   12   TDAQ IDR

Firmware

- ROD daughter card
  - Needs firmware for both eFEX and jFEX data formats
  - For the current L1Calo ROD, firmware was a major project
- Control hub
  - Smaller body of firmware needed here too
- IPMC interface
  - Hopefully not much to do here?

Software

- Online Software
  - New ATCA modules will be included in L1Calo online software
    - We already need to do this by phase 0 for L1Topo
  - Preliminary scheme outlined
    - Replace CERN VME driver and L1Calo "HDMC" (Hardware Access) by IPbus software suite developed by CMS (comes with matching firmware)
    - Keep higher level "module control" software layer in L1Calo
    - Run control layer will see common interface for VME/ATCA modules
  - We also need bit level hardware simulation (test vectors)
- Offline Software
  - New modules also need simulation in offline software
  - Used to validate trigger with P1/Tier0 monitoring
- Simulation Studies
  - Continuing work to optimise the design parameters

Schedule: Common Items

- Specification starts now/soon
  - Generally follows specification of the main modules
    - But must all be defined by the time of the TDR
- Effort: need ~16 FTE over 2013-2018 for (WP3&5)
  - Institutes: so far part of UK eFEX (4 groups) but may change

Task Name	2013	2014	2015	2016	2017
	Qtr 4 Qtr 1 Qtr 2 Qtr 3 Qtr 4	Qtr 1 Qtr 2 Qtr 3 Qtr 4	Qtr 1 Qtr 2 Qtr 3 Qtr 4	Qtr 1 Qtr 2 Qtr 3 Qtr 4	Qtr 1 Qtr 2 Qtr 3 Qtr 4
ROD					
Prototype					
Pre-Production					
Production					
Firmware					
Hub Module					
Prototype					
Production					
Firmware					
Optical Plant					
Specification					
Manufacture					
Commissioning					
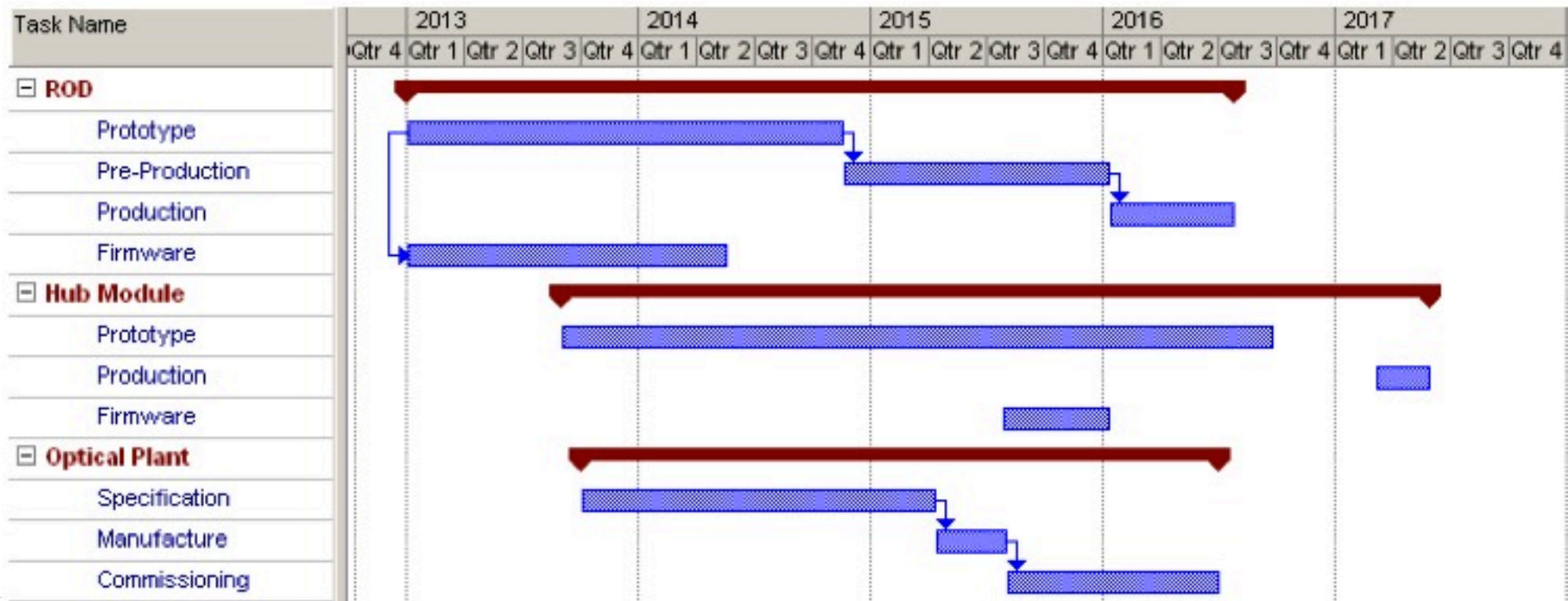
Summary & Steps to the TDR

- ## Initial design for common infrastructure exists
  - ### Detailed specification work will start soon
    - Mostly following the specification of the main modules

- ## Before the TDR we need to
  - ### Finalise mapping details soon for eFEX/jFEX design
    - Depends on decisions about BCMUX, link speeds, jet environment, etc
      - Iterative process involving LAr and L1Calo constraints - started but needs to converge
  - ### Continue tests on optical links
    - Viable link speeds, passive optical splitting etc in optical patch panel
  - ### Agree readout policy with LAr

L1Calo Work Packages

	Work Package	Effort Required 2013-2018/FTE		
		eFEX	jFEX	Total
WP1	eFEX module (h/w and f/w)	19	-	19
WP2	jFEX module (h/w and f/w)	-	17	17
WP3	ROD module (h/w and f/w)	7		7
	Hub module (h/w and f/w)	5		5
WP5	Optical plant	2.5	1.5	4
WP6	Hadronic input logic (h/w and f/w) assumes option 3	5		5
WP4	Test module (h/w and f/w)	10		10
WP7	DAQ and online s/w	11	8	19
WP8 & WP10	Offline s/w and performance studies and algorithm studies	9	9	18
WP9	Integration, installation and commissioning	15	6	21

L1Calo Overall Schedule

ID	Task Name
1	High-Speed Demonstrator Tests
2	eFEX
3	Prototype
9	Pre-Production
10	Production
11	ATCA (+TTC) module control
12	RTM: design -> commissing
13	Firmware
16	jFEX
17	Prototype
23	Pre-Production
24	Production
25	Firmware
28	JEM Daughtercard
29	Prototype
35	Pre-Production
36	Production
37	Firmware
38	PPR 80 MHz R&D
39	Test Source/Sink Module
40	Prototype
41	Production
42	Firmware
43	ROD
44	Prototype
45	Pre-Production
46	Production
47	Firmware
48	Hub Module
52	Optical Plant
56	Installation
59	System tests

Project: Master_v13
Date: Wed 12/12/12

Task	Milestone	External Tasks
Split	Summary	External Milestone
Progress	Project Summary	Deadline