DPS to FEX Mappings

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- Mappings
- HEC (EMEC fwd) options
- Optical plant (patch panels)?
- Link speed decision timetable?
- Remapping in FPGAs: resource/latency?

Basic Mapping Assumptions

- Two cases: EM layer to eFEX and the rest
- Two possible links speeds: 6.4 Gb/s or O(10) Gb/s
- Baseline 6.4 Gb/s scheme (128 bits per BC)
  - EM supercells to eFEX: two towers per link 0.2*0.1 in eta*phi
    - 20 supercells per fibre with roughly 10 bits/supercell
      - BCMUX scheme required to cope with this (not universally favoured!)
  - EM tower sums to jFEX, hadronic towers to both FEXes
    - Eight towers per fibre 0.4*0.2 in eta*phi
- Higher speed ambition (either 9.6 or 11.2 Gb/s?)
  - 192 (or 224) bits/BC at 9.6 (or 11.2) Gb/s
  - EM supercells: same 0.2*0.1 geometry, no need for BCMUX
    - Though 20 supercells in 192 bits is a squeeze
  - EM jFEX and hadronic towers: 16 towers/fibre (0.8*0.2?)
    - Fewer fibres even when increasing jFEX environment to 1.7*1.7

Interactions with LAr

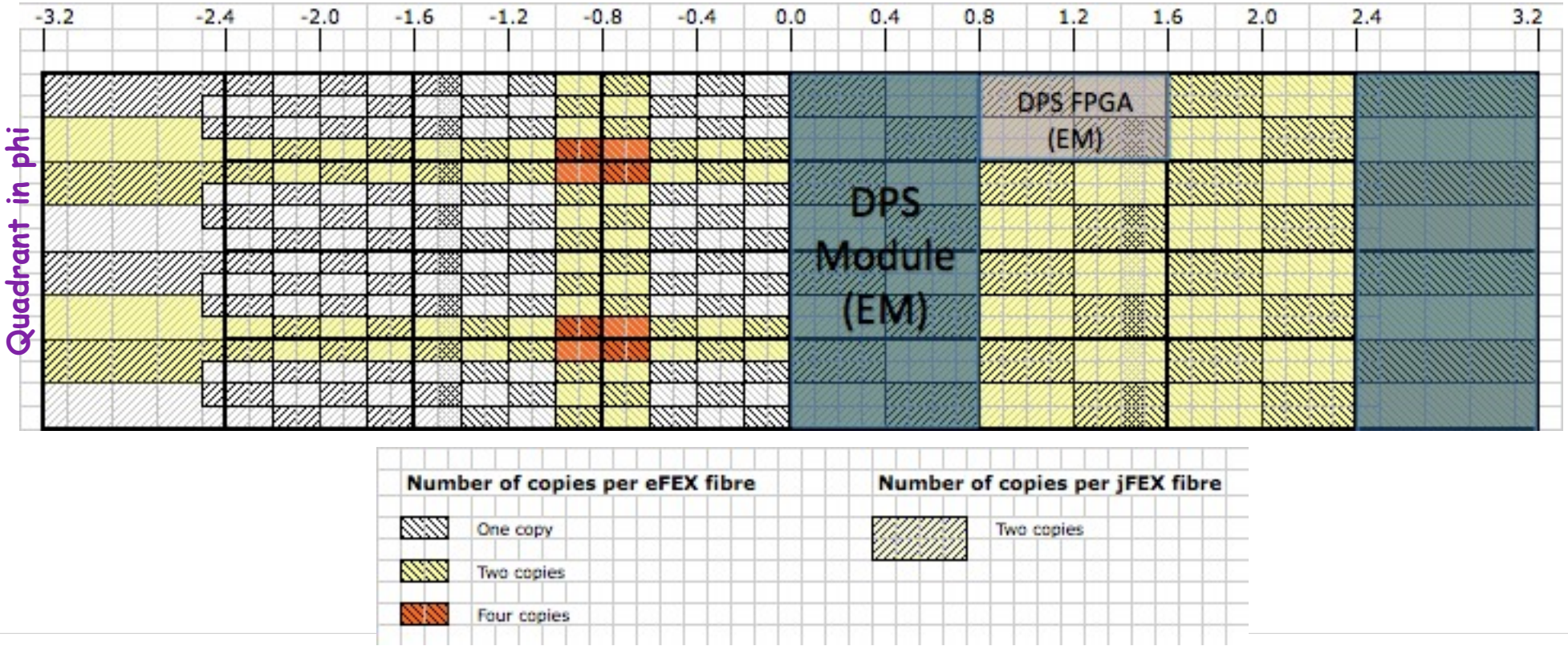
- Basic mapping layout agreed (FEX fibre geometry)
- EM barrel/endcap crack handling seems OK in DPS
  - To be confirmed after feedback from Fibernet?
    - NB extra connector & pigtails on all AMCs just to cope with overlap region
- Ongoing discussion about EMEC forward and HEC
  - Fanout for eFEX & jFEX requires inefficient use of HEC DPS
    - Or else plenty of passive optical splitting
  - Two proposals
    - Merge HEC and EMEC-forward DPS (four partly under used modules)
    - Merge EMEC-forward with EMEC-standard (making fully used modules), double up separate HEC DPS (four very lightly used modules)
    - Either could avoid need for subsequent optical splitting at 10 Gbit/s

DPS Fibre Outputs EM (1)

- Diagrams from set of spreadsheets…
  - Shown for one quadrant

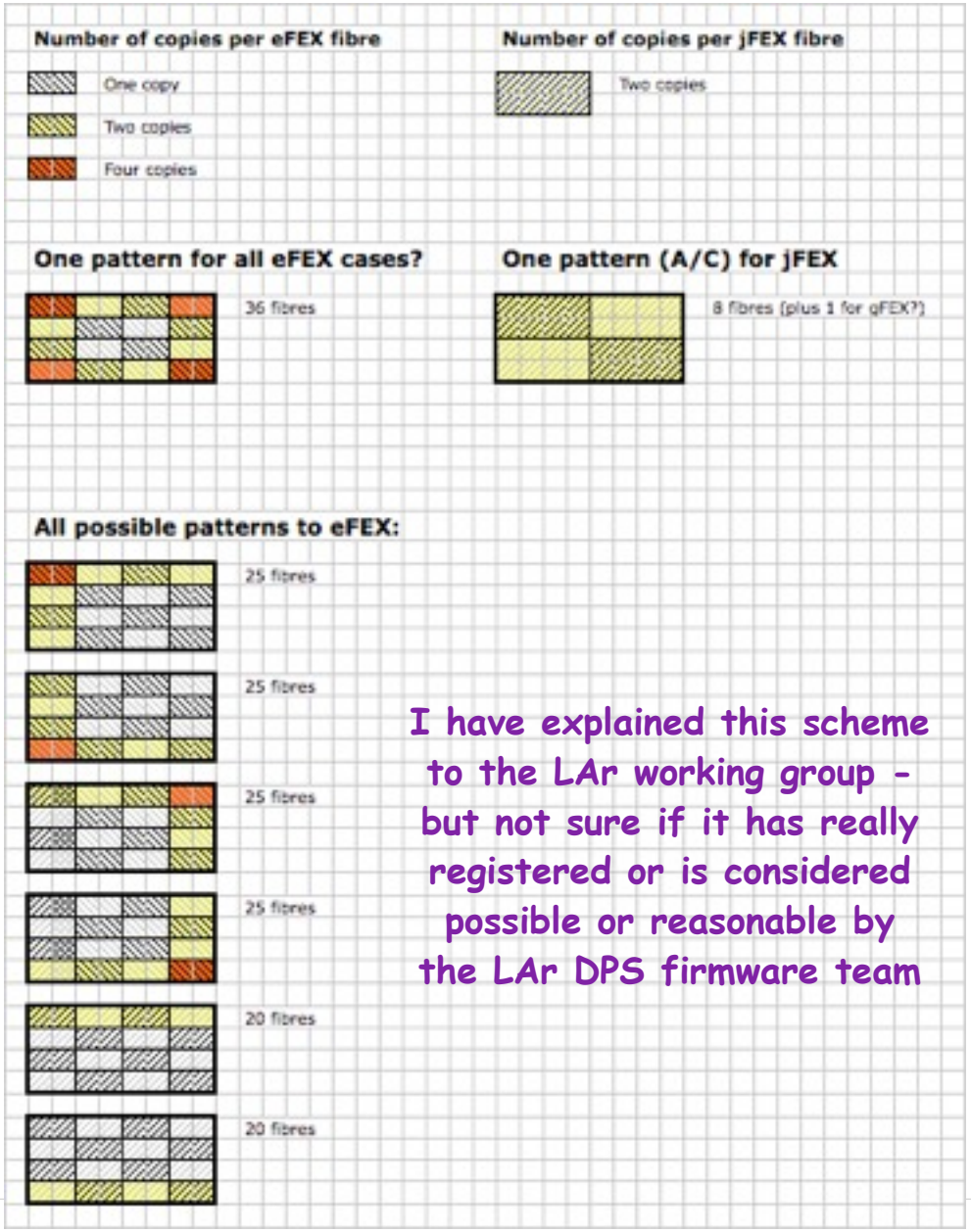
Fibre Outputs to eFEX
(Left side of diagram)
Several patterns:
extra fanout at corners

Fibre Outputs to jFEX
(Right side of diagram)
Simple pattern:
two copies of everything



DPS Fibre Outputs EM (2)

- Aim for single firmware for central EM DPS
  - OR of the six different eFEX patterns
  - Uses 36 outputs (no more than 25 needed for any single pattern)
    - Switch off unused outputs to save power
  - Also 8 outputs for jFEX
    - Only 6 at 10 Gbit/s (each fibre covers twice the area but three copies for 1.7*1.7 jets)
  - 1 output for gFEX
  - Total 45 (of 48 available)



I have explained this scheme to the LAr working group - but not sure if it has really registered or is considered possible or reasonable by the LAr DPS firmware team

DPS-FEX Optical Plant

- Least understood part of the system?
  - At least by me!
- Will there be any unexpected constraints from it?
  - Number of optical connections, impact on optical power?
    - Depends on link speed and need (if any) for passive (or active?) splitting
- Helpful to have a "strawman" design for this soon
  - How modular can we make it?
  - How hard a limit is the separation of each AMC on the LDPBs?
    - No mixing of ribbons between AMCs due to front panel and desire to be able to easily replace one AMC
  - Interaction between optics and AMC remapping capability
- MSU proposes a planning discussion soon...
  - Intention to test full optical path at MSU
    - Connectors, splitters (if needed)

Testing and Commissioning?

- Procedures for testing the installation
  - Current L1Calo runs test vectors through the digital system
  - Compare results against the expected connectivity (in DB)
  - Also check for algorithmic correctness and link errors
- Extend this to DPS in some way?
  - Connectivity: send self-identifying patterns from DPS
  - (PS is something like this foreseen from LTDBs?)
- Need to start talking about software sometime...

Link Speed Decision?

- Many things depend on link speed choice
  - Number of output fibres (more towers/fibre)
  - Possible jFEX environment
    - Baseline 0.9*0.9 jets at 6.4 Gbit/s or 1.7*1.7 jets at ~10 Gbit/s
      - Consequent impact on the case for a gFEX
  - Detailed mappings
    - DPS output arrangement for all tower fibres
    - In particular choice of DPS HEC/FwdEMEC arrangement
      - At higher speeds some arrangements can avoid any subsequent optical splitting
  - Work on filters
    - Wiener filter only appropriate if no BCMUX
- How long do we need to carry both options forward?
  - L1Calo (eFEX) view: until eFEX module prototype shown to work at O(10) Gbit/s - scheduled for some time in 2015

Remapping in DPS AMC FPGA

- LAr TDR states "remapping in DPS is easy"
  - I hope this is really true
  - Would be good to estimate the FPGA resource impact of remapping DPS AMC inputs to output patterns for FEXes
- Are different firmware variants required?
  - Surely need several radically different remappings
    - EM barrel, EMEC standard, EMEC special + HEC, FCAL
  - Do these need different DPS AMC firmware bit files?
    - If so, would LAr have a scheme to load the right one automatically?
  - Or can the remapping be configured (without latency impact!)

Summary

- Mapping discussions with LAr ongoing
  - Basics agreed (and well defined for standard EM part)
  - Various ideas for handling HEC and forward EMEC
  - Need to estimate impact of remapping on firmware resources
- Early decision on link speed desirable
  - Otherwise we have to keep multiple options alive
- We need a clearer picture of what the optical plant is going to look like…
- Meanwhile start writing a mappings document