TBB-DPS-FEX Connectivity

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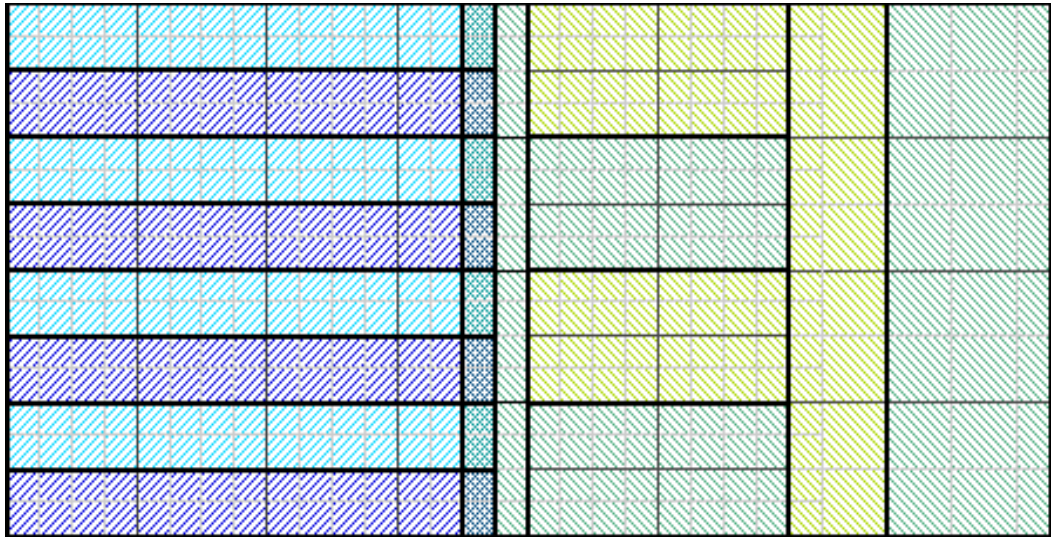
23 April 2012

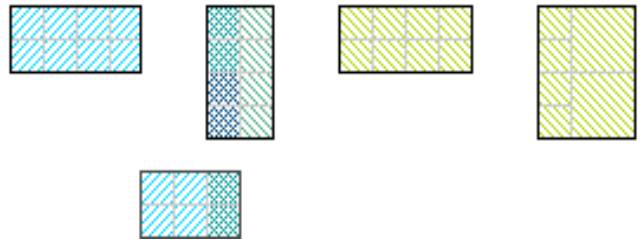
- TBB layout & fibres?
  - Overlap region
  - 1341 region
- DPS layout?
- eFEX layout?
- Assumptions and open questions

TBB Layout

- TBB: up to 32 towers
  - Various geometries
- dTBB: assume 1:1 map?
  - LAr like mezzanines
  - 4 mezzanines/dTBB
  - 8 towers per mezzanine
    - 80 supercells (1441)
  - ADC: max 12 bits?
    - 80*12 = 960 bits
    - LAr aim for 10 Gbit/s
    - Need 5 out of 12 fibres
      - Say 6 with one redundant
      - SNAP12 half used

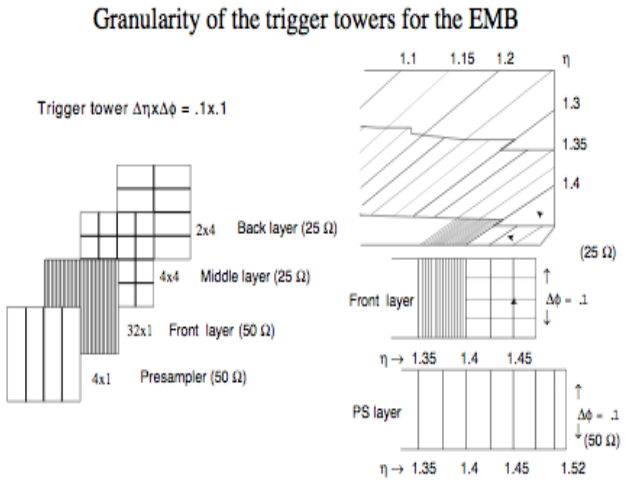


dTBB Mezzanines (8 towers, 80 supercells)



Overlap Region (1.4 < |eta| < 1.5)

- Barrel component: 1001
  - Presampler
  - "Barrel end": Sum of ~3 front + 1 middle
    - "Barrel end" handled by back layer FEB
- Endcap component: 0140
  - Front: low granularity => 1 supercell
  - Middle: 4 supercells as elsewhere
- Merging to 1141?
  - Can 5 fibres per dTBB mezzanine be grouped as:
    - 1 fibre for PS + back, 2 fibres Front, 2 fibres Middle?
  - If so may be able to merge overlap region as 1141 into DPS
    - Assumes there could be fibre patching between dTBB and DPS
    - And might lose any redundancy in fibres from dTBB?

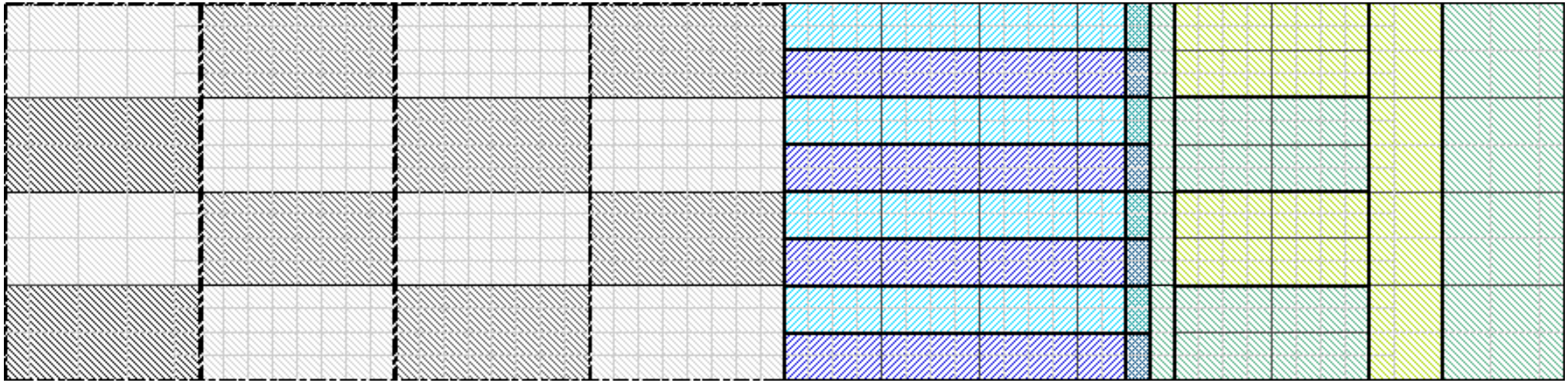


1341 Region (1.8 < |eta| < 2.0)

- Two eta bins per endcap have 24 strips per tower
  - Gives six sums of four cells from the shaper
  - LAr suggests providing equal width 3 supercells here
    - Excel spreadsheet from Hucheng Chen [CHECK]
  - I wonder if we would prefer four unequal width supercells?
    - Eg 0.016, 0.033, 0.033, 0.016
    - If thats feasible in the layer sum board...
  - (Assuming we want the 1441 option in general)

DPS Layout?

- LAr still like mezzanines...
  - Suggested design has 4 mezzanines on one ATCA carrier
    - Mezzanine (toy layout?) has four minipods and one FPGA
- Inputs: two 12 fibre ribbons?
  - Regroup two half used dTBB SNAP12s to one DPS SNAP12?
  - One DPS mezzanine handles four dTBB mezzanines?
    - If so, one mezzanine handles 32 towers, eg 4*8 or 8*4 shape

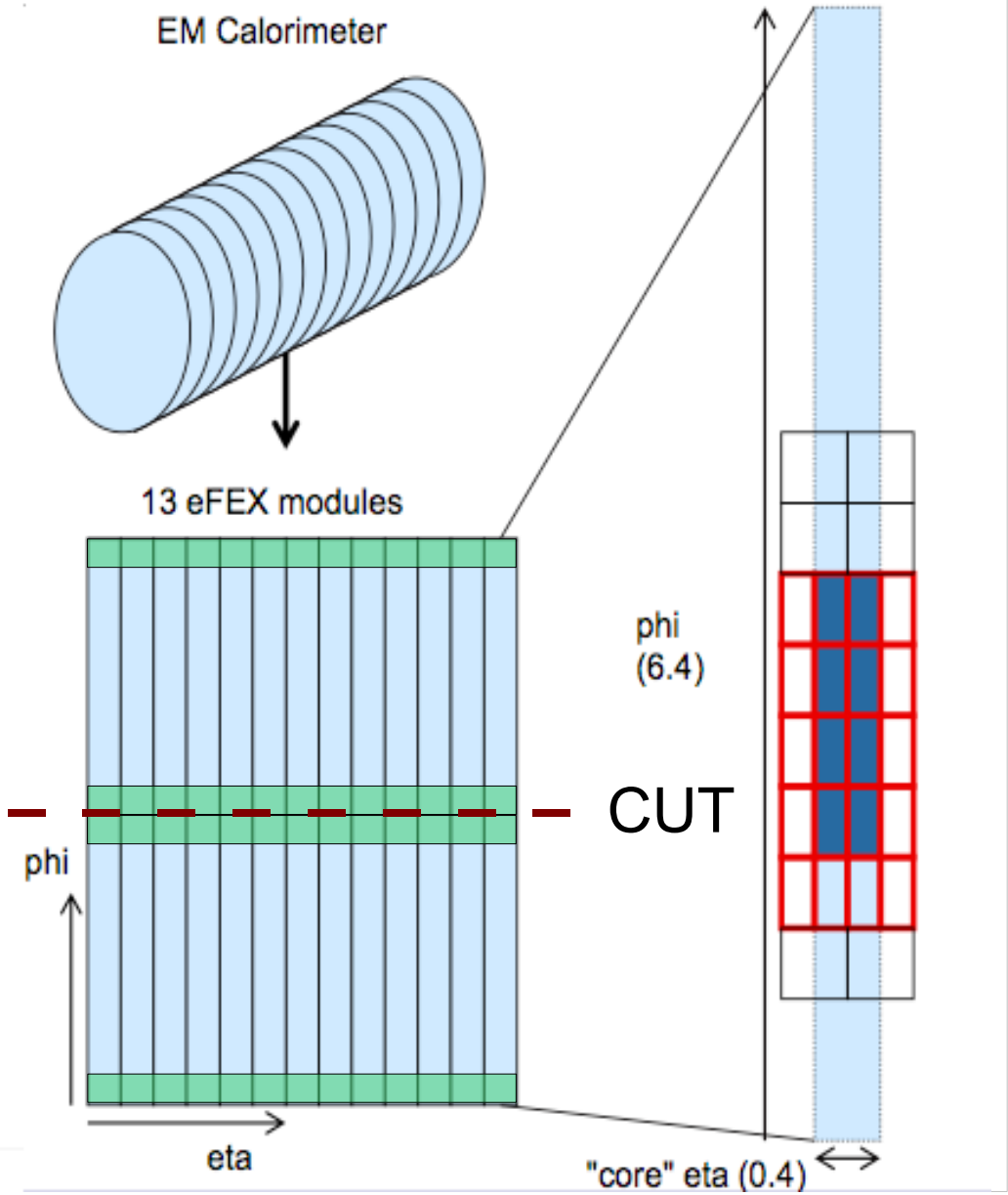


DPS Output?

- Bandwidth: output >= input
  - BCMUX halves output bandwidth (to eFEX)
    - But duplication at source doubles it, also need output to jFEX
- DPS mezzanine: two input and two output minipods?
  - If 100% duplication, have one minipod (12 fibres) "core" out
- Output to eFEX
  - "Sam scheme" has 8 towers on 3 fibres
    - Assumes 1141 if 6.4 Gbit/s links, or 1441 if 10 Gbit/s links
    - Need 12 fibres for output to eFEX: no room for jFEX!
      - Unless we have less than 100% duplication: can we find a geometry that works?
- Output to jFEX
  - "Sam scheme": 16 towers/fibre => 2 "core" fibres/mezzanine
    - Any way to group jFEX outputs at the module level?

eFEX Layout?

- What is the maximum input per module??
  - Even Sams two crate scheme is considered too dense
- Cut Sams single crate scheme in half at eta=π
  - Needs 25% passive optical fanout (as well as 100% duplication at source – at least for 4*4 or 5*5 environment)
  - More modules but matches dTBB/DPS geometry?



Assumptions and Open Questions (1)

- Assume we will never want EM triggers for |eta|>2.5
- Never want finer than 0.2 granularity in inner EMEC?
- Assume all fanout is optical: is that totally definite?
- Link speeds between DPS and eFEX/jFEX
  - Does 6.4 vs 10 Gbit/s choice determine 1141 vs 1441
  - Or do we need to work out a 1441 geometry for 6.4 Gbit/s?
  - Impact on DPS design if it has 10 Gbit/s in but 6.4 out...?
- Environment size for eFEX?
  - 0.3*0.3 reduces required optical fanout – but feels too small
- Data content of links?
  - Do we need more than Et (precise time, pulse quality, sumE)?

Assumptions and Open Questions (2)

- Granularity of jFEX?
  - 0.1*0.1 vs 0.2*0.2 has big impact on DPS output to jFEX
  - When do we need to make a decision on this?
- Maximum granularity from present FCAL for jFEX?
  - Allowance for inputs from future new FCAL
- Eta phi geometry of phase 2 Tile RODs
  - Affects possible geometries of hadronic fibres already now
- Density of ATCA modules...
  - LAr designs (16 minipods @ 10Gbit/s + 4 FPGAs on 4 mezzanines per module) seem more ambitious than ours?