L1Calo Phase 1

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(shuffling slides from colleagues in a new order)

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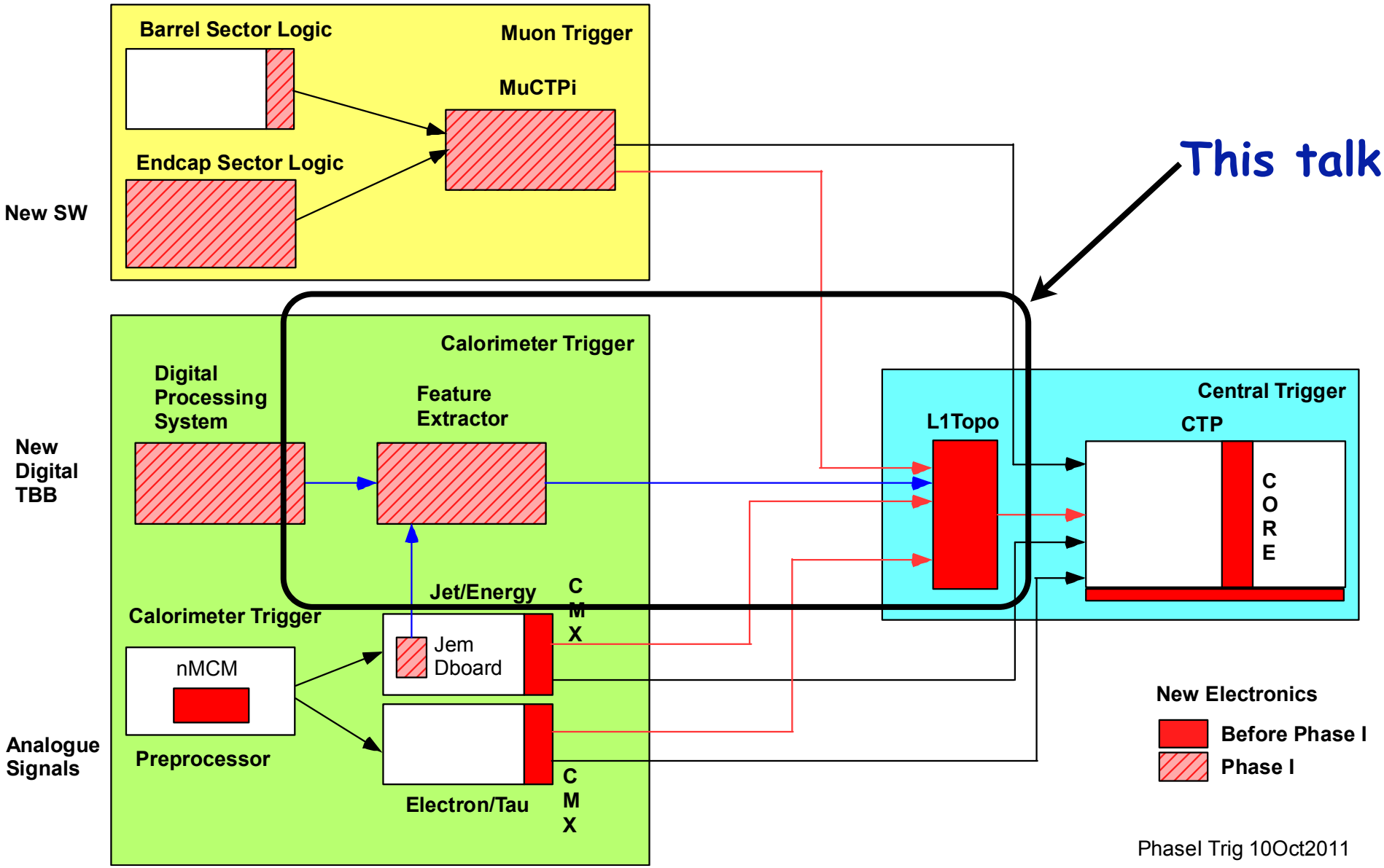
- Overview
- Current status of eFEX & jFEX
  - And L1Topo
- Interface with DPS

Introduction

- Recent L1Calo technical workshop (Feb)
  - Lots of useful discussion, different schemes presented
    - https://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=172073
  - Updates at recent mini TDAQ update week
    - https://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=165240
  - Some consensus, but still plenty of things to sort out
    - Ideal scenarios vs practical constraints
    - Ambitious vs conservative designs, etc
- Show current status of L1Calo phase 1 plans
  - Health warning: diagrams are illustrative not final!
    - Some personal choices of what to show in limited time
    - Work is still in progress, both within L1Calo and with calorimeters

Overview of L1 at Phase 1



Overview of L1Calo at Phase 1

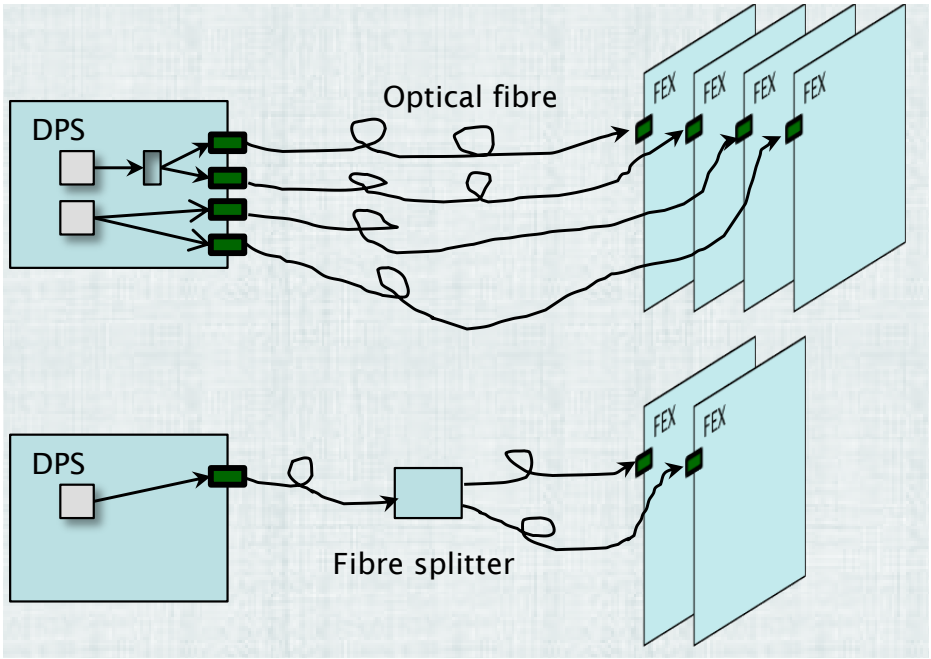
- Keep existing system handling analogue signals
  - Minimise risk (if possible) until phase 2
- New EM/Tau and Jet feature extractors (eFEX/jFEX)
  - Separate processors for EM/Tau and Jet/Energy
  - New fine granularity EM signals from "digital TBB" and DPS
    - Also summed into coarser granularity for jet algorithms
  - Still get hadronic signals (Tile+HEC) from current L1Calo
    - NB requires faster transmission from Preprocessor (new MCM)
    - And optical outputs from new daughterboard on current JEMs
    - Will need DPS (or similar) for HEC and FCAL in phase 2 (and Tile RODs)
- FEXes feed results to topological processor (L1Topo)
  - L1Topo will exist ~from phase 0
  - Add additional board(s) for phase 1?

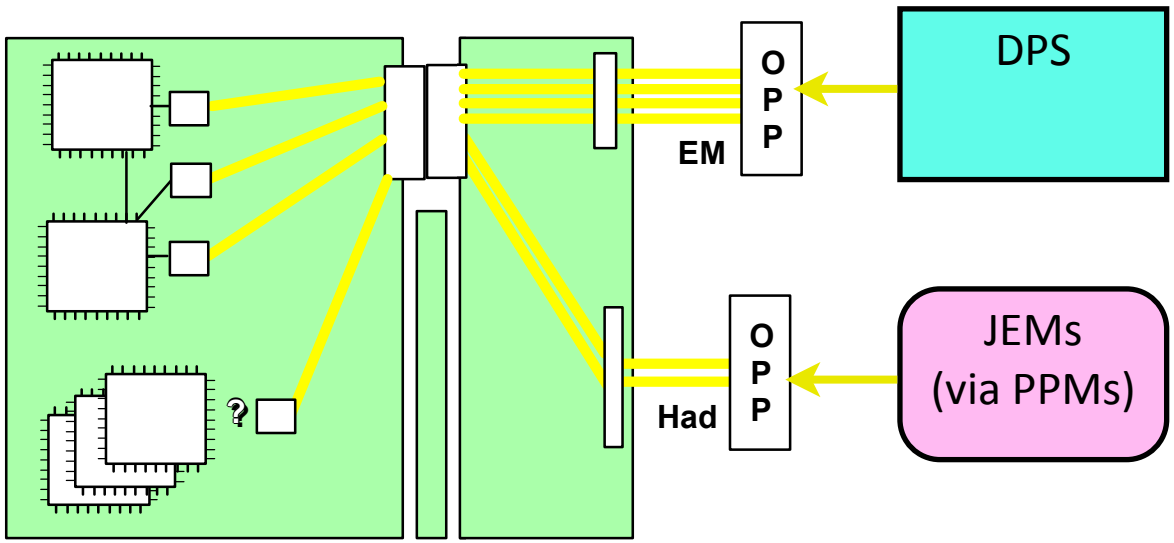
FEX Design Issues

- Best algorithms and their "environment"
  - eFEX: 0.4*0.4 is fine for EM, 0.5*0.5 modest benefit to Tau
  - jFEX: 0.9*0.9 minimum for jets, larger would be better
- Fanout implications of chosen algorithms
- Reliable data transmission on & between modules
  - Optics all the way to (near) each FPGA
  - Can use "far end loopback" to duplicate data between FPGAs
- Maximum number of fibres per module (~140-180?)
  - Using ATCA zone 3 for optical connectors from RTMs
- Link speeds: stick to 6.4Gbit/s for now
- Data content on links: granularity, precision
- Organisation of links to FPGAs, modules & crates
- Impact of L1Calo requirements & choices on DPS...

Optical Transmission Scheme

- Need reorganisation of signals between DPS & FEX
- Also need to minimise number of optical connections to reduce optical power budget
- Duplication at source favoured over splitting
- Route fibre bundles directly to rear zone 3 connector
  - Rear transition module (RTM) only used for cable management
- On board fibre pig tails to "miniPODs" near FPGAs
- Can make one electrical copy to adjacent FPGA
- No long links to adjacent modules via backplane

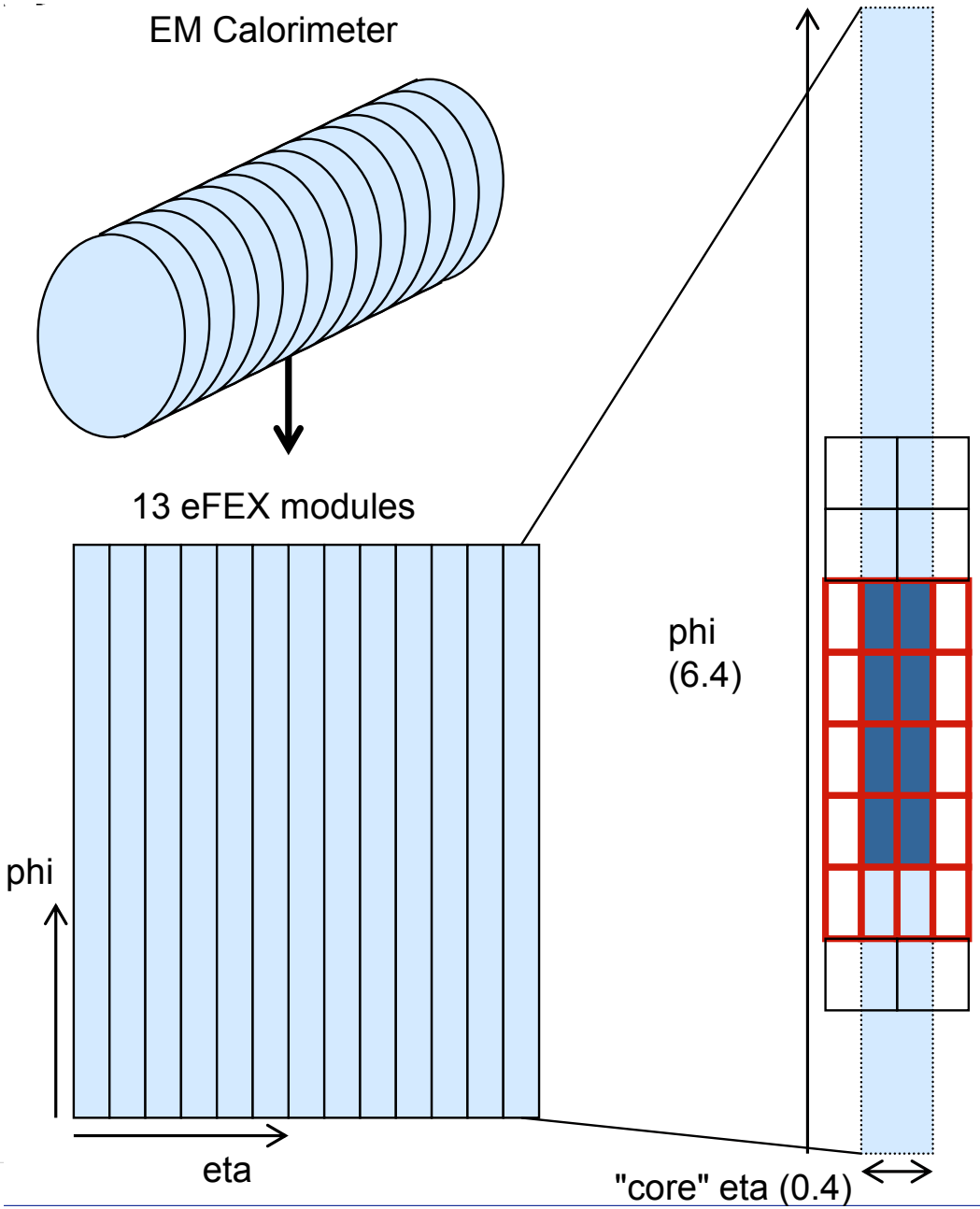




eFEX

- Some appealing designs (next slides)
  - Nice geometry, compact, simple mapping to DPS, no additional passive optical splitting
  - However, even two crate version has more fibres per module than our engineers are comfortable with
    - Unless the technology improves a lot fairly soon
- Alternative schemes with fewer fibres/module
  - Tend to have less attractive geometry, more complex mappings, perhaps 1:4 fanout from DPS, etc.

eFEX: Single Crate (Ambitious!)



Hadronic "group" 0.4 x 0.4
(1 fiber, 16 towers)

EM "group" 0.2 x 0.4
(3 fibers, 8 towers)

eFEX module "core" (0.4 ring in eta)

"core" coverage of one FPGA
(0.4 x 1.6)

One FPGA receives:

15 EM "groups"	(45 links)
10 hadronic "groups"	(10 links)
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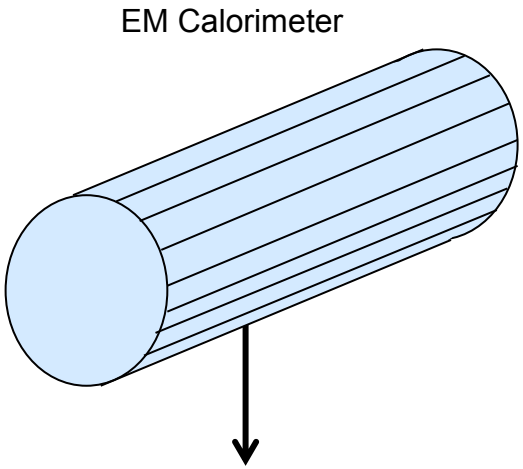
Total	55 input links

eFEX: Two Crates

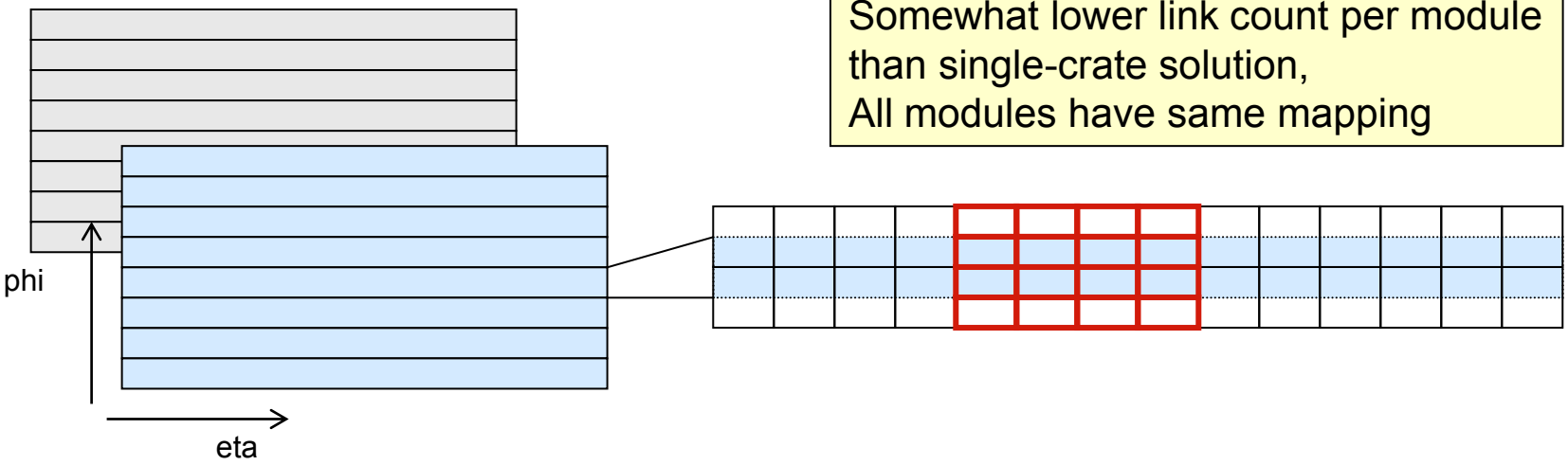


Hadronic "group" 0.4 x 0.4
(1 fiber, 16 towers)
28 fibers per eFEX module

EM "group" 0.2 x 0.4
(3 fibers, 8 towers)
168 fibers per eFEX module

eFEX module (0.4 strip in phi)

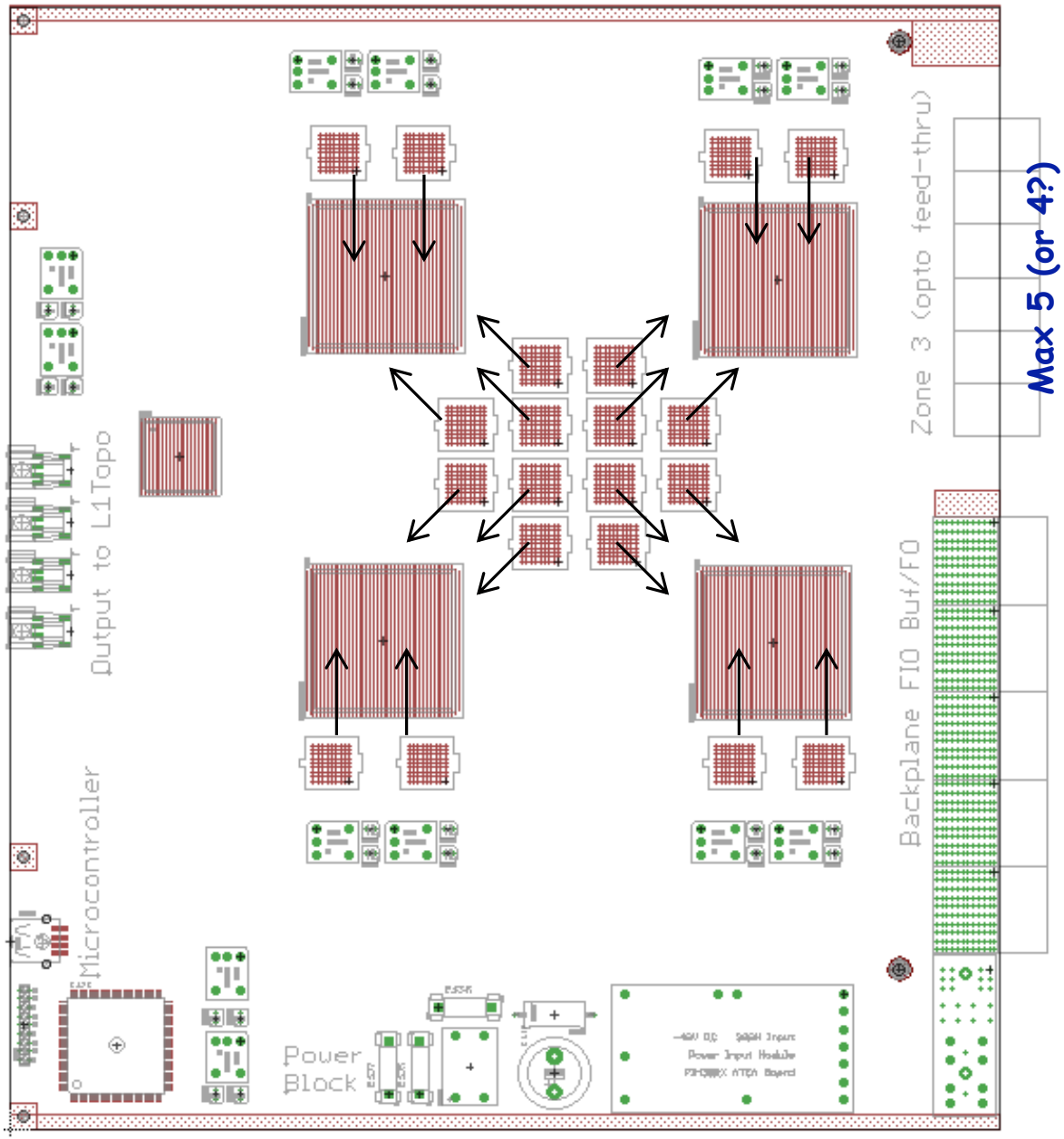
168+28=196
Still too many for comfort...



Somewhat lower link count per module than single-crate solution,
All modules have same mapping

Alternative two crate solution: Cut previous one crate scheme in half at phi=pi with small region needing 1:2 passive optical splitting

eFEX Module: Toy Layout

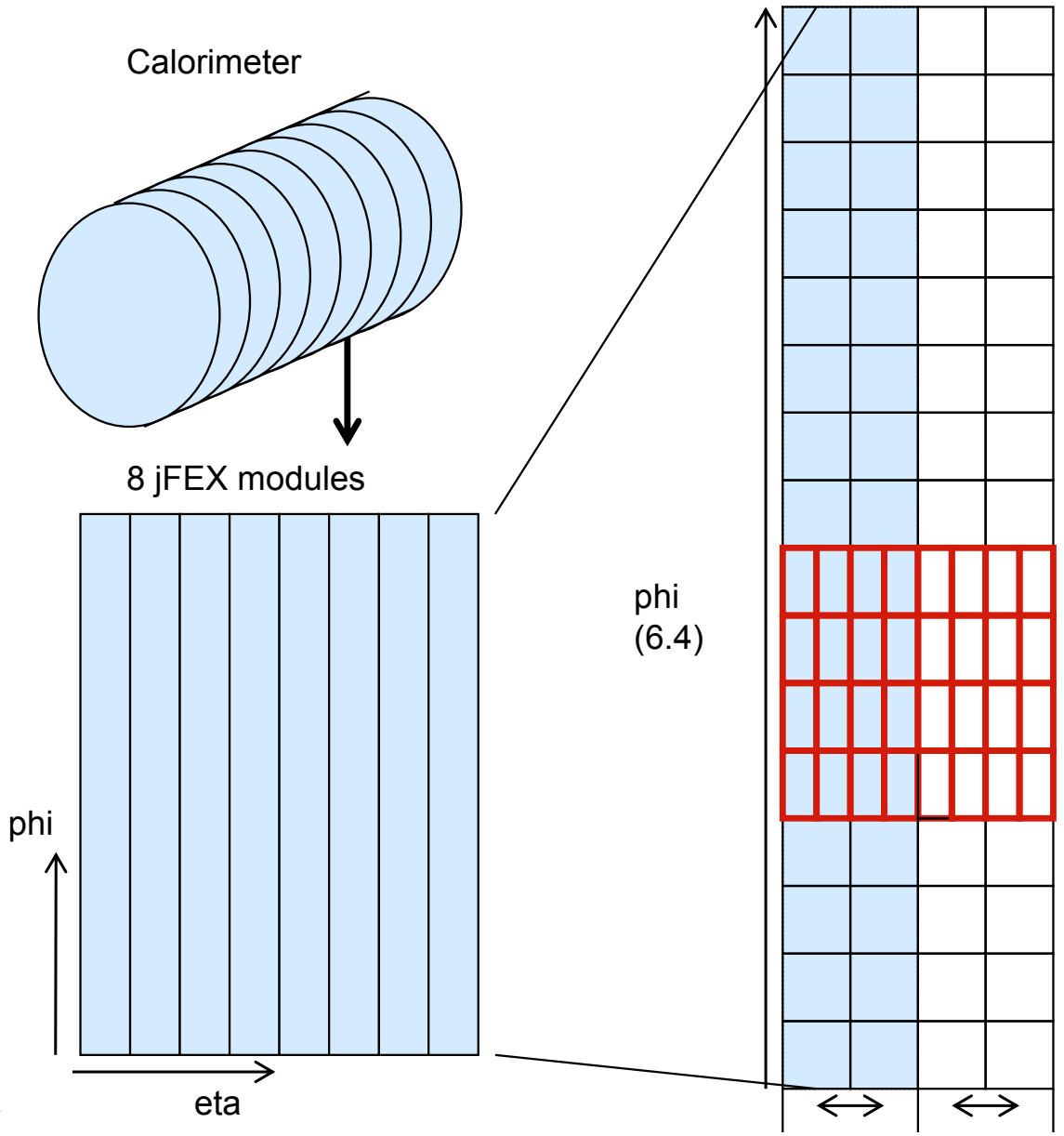


- Example: one-crate eFEX
- One FPGA per quadrant
- Five MiniPOD receivers per quadrant
  - Four EM
  - One Hadronic
- Fifth, smaller FPGA for merging

jFEX

- Original idea to use 0.1*0.1 granularity for jets
  - Slide window by 0.1
  - Fanout and FGPAs limit jet window to about 0.9*0.9
  - Would ideally like a bit large jet windows than that
- Recent studies (Alan)
  - Most benefit to jets from digitisation at fine granularity
  - Also smaller quantisation scale (0.25 GeV)
- Starting to wonder if we should stick with 0.2*0.2 jets
  - Much reduced bandwidth
  - Could "easily" have larger jets, eg 1.2*1.2

jFEX: Example Design



Hadronic "group" 0.4 x 0.4
(1 fiber, 16 towers)
64 fibers per eFEX module

128+64=192
Bit too many
for comfort...

EM "group" 0.2 x 0.4
(1 fiber, 8 towers)
128 fibers per jFEX module

jFEX module (0.8 ring in eta)

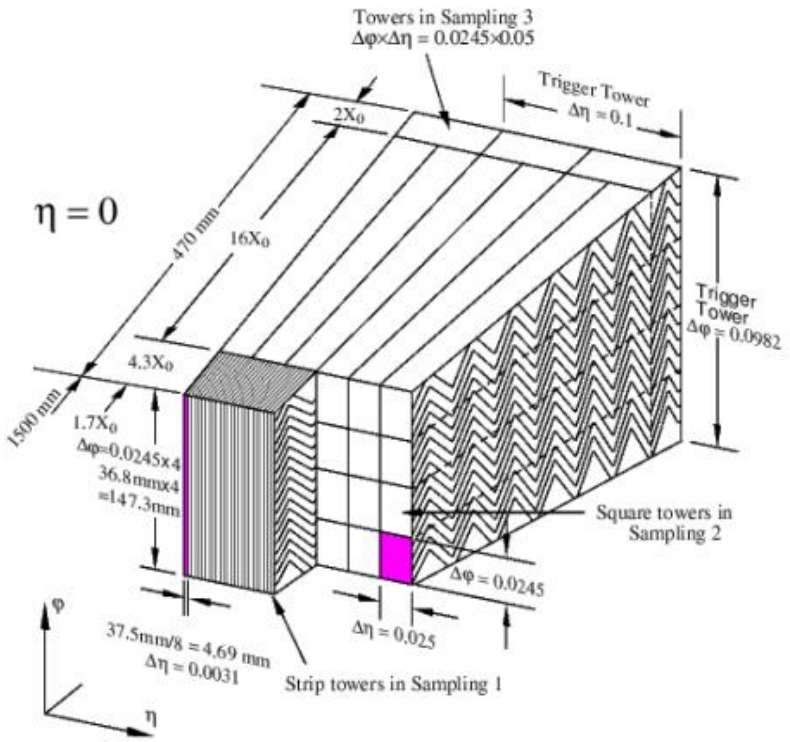
Progress and Plans

- UK High Speed Demonstrator module
  - Test ability to handle many variants of high speed links
  - Due this summer: lessons learned will feed into eFEX design
- Planning for the eFEX
  - Serious project planning started
    - In parallel to continued design studies
  - Trying to assign responsibilities for HW and firmware
    - (Still need to think about software)
  - Need to bid for funding soon
- jFEX
  - Design studies continuing
    - In parallel with higher priority work on L1Topo

L1 Topological Processor

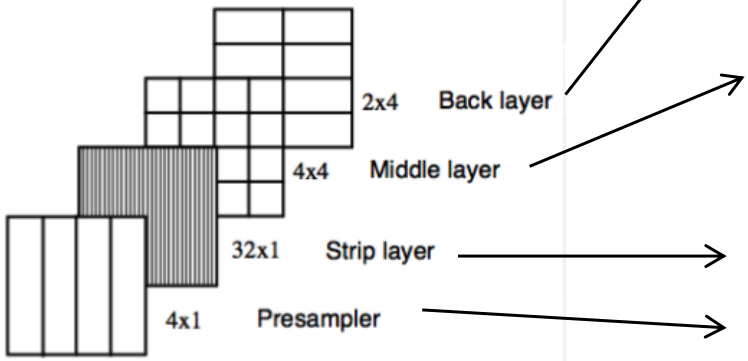
- Initial L1Topo is to be installed before phase 1
  - Designed as a modular system
  - Initially taking input from phase 0 CMX modules
  - For phase 1, additional L1Topo module(s) will take input from eFEX and jFEX modules
  - If we need more algorithms, we can add more modules
  - For phase 2, one L1Topo module (by then renamed as L0Topo) could provide L0 RoIs to the L1 track trigger
- Progress and plans
  - Lots of thought & simulation of algorithms (talk by Jim)
  - Demonstrator module (GOLD) is currently under test
  - Prototype L1Topo currently being designed
  - Installation expected in 2014

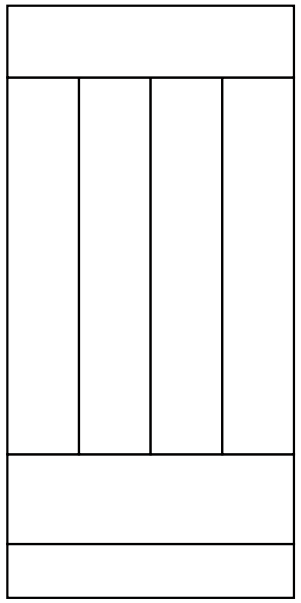
Interface with DPS (1)

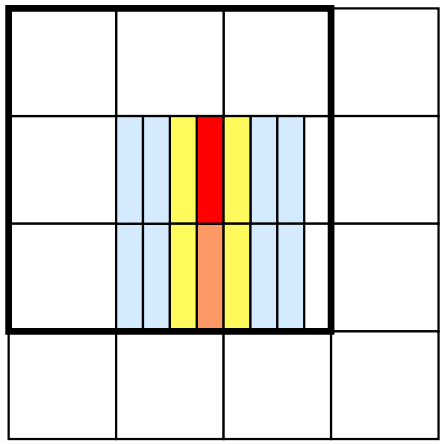


For 6.4 Gbit/s and 7 sums/tower, eight towers can be sent to eFEX with 3 fibers.

Baseline:
7 sums/tower







Baseline: 1 PS, 1 Front 4 Middle, 1 Back layer: 1-1-4-1

1-4-4-1 later?
(not favored)

Interface with DPS (2)

- Small group discussing with calorimeter colleagues
- FEX requirements on the DPS:
  - Digitisation, BCID, calibration of signals
  - Output of high/low granularity signals to eFEX and jFEX
  - Optical duplication of signals at source
    - Typically 1:2, perhaps some 1:1, maybe some 1:4 required
  - Reorganisation of signals on fibres
    - Especially to smooth out the barrel/endcap boundary
      - NB may not be able to have 4 middle layer signals in the overlap region (1-1-1-1, not 1-1-4-1)
      - This means the eFEX will have to run the "legacy" algorithm in that region
- Need to iterate link organisation between DPS & FEX
  - My recommendation: 100% duplication of signals with high optical power (to allow fibre rebundling and 1:2 passive optical splitting) gives maximum decoupling between DPS and FEX geometries

DPS/Tile Interface at Phase 2

- Phase 1 eFEX/jFEX should be compatible with phase 2
  - Will be the L0Calo processor in phase 2 architecture
- Make reasonable assumptions NOW for phase 2 needs
  - But these then become fixed constraints!
- Assumptions/questions:
  - Never want EM/Tau at |eta|>2.5?
  - Never want finer than 0.2*0.2 granularity from inner wheel?
  - Maximum granularity from present FCAL?
  - Maximum bandwidth from any new FCAL?
  - Eta-phi geometry of phase 2 Tile RODs?
  - Will we want same hadronic granularity for eFEX and jFEX?
    - For phase 1 we cannot have depth info for eFEX, for phase 2 we could
  - Content & bandwidth of links: need anything more than Et?
    - Eg precise time, SumE?

Summary

- L1Calo plans for phase 1 progressing
  - Many technical details discussed at recent workshop
    - Consensus reached on some aspects
  - FEX designs still evolving…
  - Detailed planning started for hardware and firmware projects
  - Demonstrator modules under test or coming soon
  - Simulation studies reaching conclusions
  - Discussions with calo groups ongoing…