L1Calo Upgrade Phase 2

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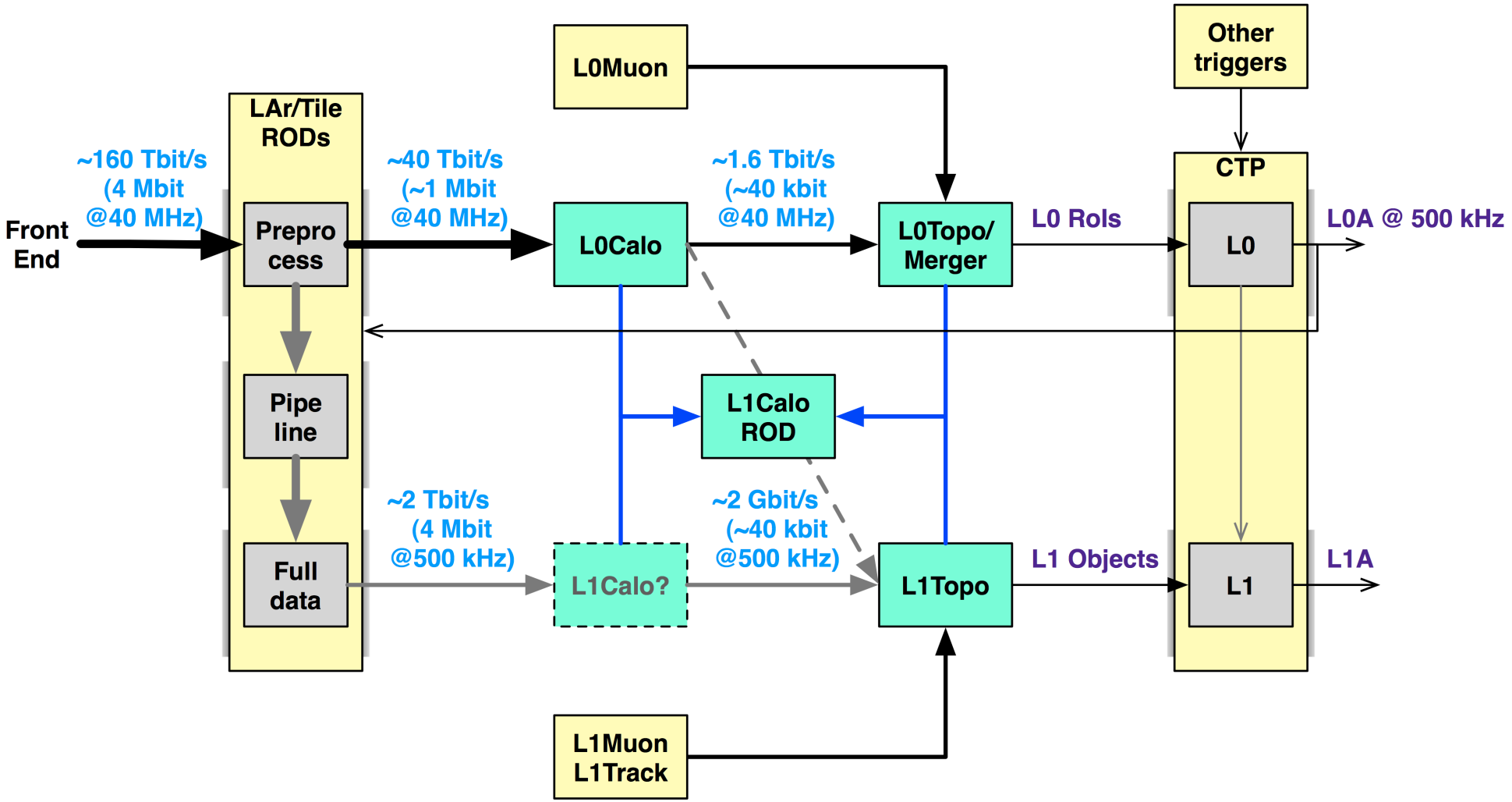
L1Calo Phase 2 Introduction

- Assumes replacement of calo front end electronics
  - Fully digital system, no analogue signals for the trigger
- Every calo cell digitised on detector and transmitted to new calo RODs every bunch crossing (160 Tbit/s)
- Calo RODs preprocess the digitised pulses
- Extract Et, assign to correct bunch crossing
- Perform some summing of cells to "mini towers"
  - Finer granularity (eta, phi, depth) than the present trigger
- Transmit mini towers to L1Calo (~40 Tbit/s?)
- Require minimum latency
  - New RODs to be located next to new L1Calo in USA15

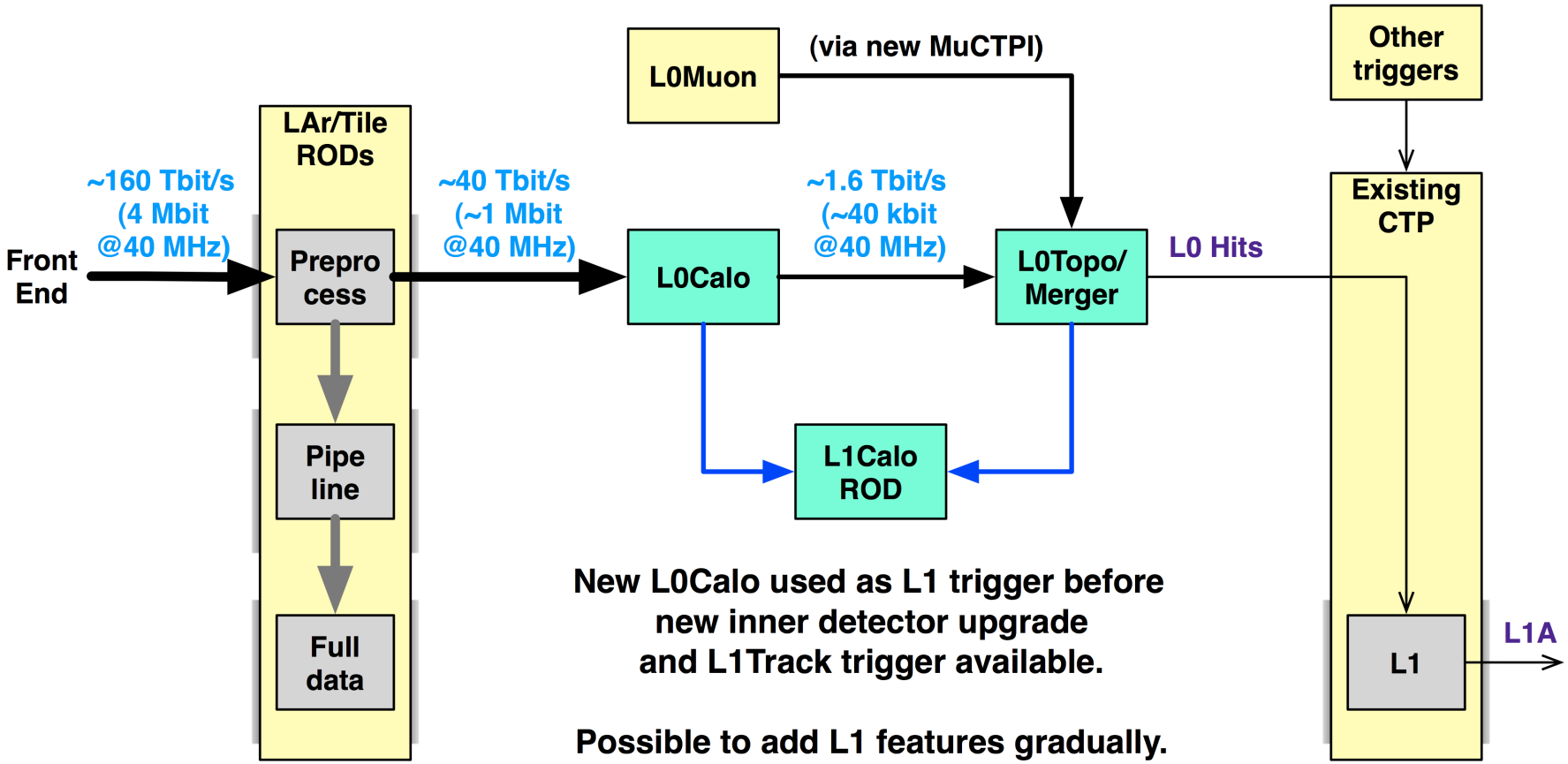
Scenarios: Level 0 and Level 1?

- Probably split present L1 trigger into L0 and L1 stages
  - Required for the regional (RoI seeded) L1Track trigger
  - Not necessary for the standalone L1Track trigger
    - Unless there are permanent latency constraints from muons
- Latency requirements
  - For regional L1Track, need L0 RoIs in USA15 within 2-3μs
  - Present muon readout needs L1A on detector within 3μs
- Likely scenario:
  - New L0Calo + L0 topological processor + L0 CTP
    - Provides L0Accept and L0 RoIs within about 2.5μs
    - Compatible with regional L1Track and existing muon readout
    - Possible L1Calo stage refining L0 decision in parallel with L1Track
- Less likely?
  - New single stage L1Calo in parallel with standalone L1Track

L0/L1Calo Functional Block Diagram?



Phase 2B: New L0Calo Used as L1



L0Calo System

- Receive ~40 Tbit/s from new calo RODs
  - Up to 200 bits per 0.1*0.1 EM tower per BC, 25 bits hadronic?
- Baseline architecture: phi octant system
  - Eight ATCA crates each handling all eta for one octant in phi
  - Single processor module (~8 per crate) for EM/tau/jets
    - Might need separate jet processor if bandwidth per FPGA is limited
  - Sliding windows with fine granularity (eg 0.05*0.025?)
    - Import algorithms from current level 2
- Results each BC to L0 topological trigger
- Readout via new (L1Calo) RODs in the same crate
- Used as input to L1 trigger before ID upgrade

L0 Topological Processor

- Receive ~1-2 Tbit/s from new L0Calo
  - Also inputs from new MuCTPI
    - Present (or upgraded?) RPC/TGC triggers rebranded as L0Muon
- Similar architecture/design to phase 1 TP proposals
  - Phase 1 TP could be prototype of phase 2 version
    - Or already the final one?
- TP modules running variety of topological algorithms
  - Input data fanned out optically => scalable system
  - Readout via new common L1Calo ROD
- Outputs:
  - L0 trigger items to CTP
    - Could be existing CTP until ID upgrade and L0/L1 trigger split?
  - L0 RoIs to future L1Track trigger
    - Maximum expected L0Accept rate of 500 kHz

Possible L1Calo Stage (After L0)

- Possibility of L1 refinement of L0Calo trigger
  - Only in the scenario with separate L0 and L1 triggers
- LAr/Tile RODs pipeline **full** granularity data
  - Et and time for every cell
  - Full LAr strip data available: good for π0 rejection
- Send to L1Calo stage on receipt of L0Accept
  - Rate <500 kHz, one L0A every 2μs
  - Roughly 4 Mbits per L0A => 2 Tbit/s average (derandomised)
- Refine original L0 RoIs with full granularity data
  - Could run full L2 calo algorithms – if possible in firmware?
- Output L1 results to L1 topological processor
  - Readout via new common L1Calo ROD
- Single ATCA crate system?

L1 Topological Processor

- Receives L1 results at L0Accept rate (<500 kHz)
  - Calo, muon and tracks
- Runs more sophisticated algorithms than L0Topo?
- Otherwise similar architecture
  - At lower data rate
- Output to new CTP
  - And to new level 2?
- Readout via new common L1Calo ROD
- Single ATCA crate system

Latency

- New L0 trigger latency limited to 2.5μs (in USA15)
  - Less than 3.2μs back on the detector
- Early LAr estimate: ~1.0μs (40BC) up to ROD outputs
  - Includes ~70m fibres from detector (0.35μs)
- Subsequent cable/fibre paths:
  - 15m ROD-L0Calo, 10m L0Calo-Topo, 5m Topo-CTP: 0.15μs (6BC)
- Serialisation/deserialisation
  - Expect ~5BC (0.125μs) per stage (using custom chips?)
    - PROBLEM: Tile measured up to 0.4μs in FPGA implementation
  - Need FE-ROD, ROD-L0Calo, L0Calo-Topo, avoid to CTP?
  - Three or four (de)serialisations => 0.4μs (15BC)
- Logic: L0Calo+L0Topo+CTP
  - Left about 1μs for algorithms in firmware...

Timescales

- Phase 2 timescale not yet clear
- If 2017, no time (no point?) for phase 1 upgrade
  - Go straight to phase 2
  - Need to start serious work ASAP!
    - Efforts up to now concentrated on phase 1
- If later, phase 1 may still be useful
  - Treat topological processor as prototype for phase 2
- Need a decision on phase 2 timescale soon
  - Which is adhered to (+- about a year)

Rough Planning

- Time for removal of existing L1Calo (and calo FE) and installation of complete new system will be short
  - Need full system ready and tested 1 year beforehand
  - One year for production and module testing
  - One year for final prototypes & system tests, reviews
  - One year for final design work, start system tests
  - One year for early prototypes, technology choices
  - One year for simulation studies and technology R&D
- Need at least six years from now to installation
  - 2017 is the earliest reasonable date but should be possible

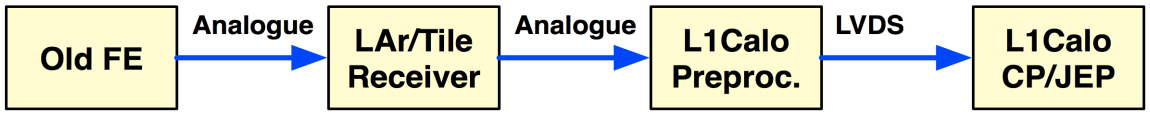
Installation Logistics

- Remove existing L1Calo and Receiver system
  - Mass of underfloor analogue and LVDS cables
  - Long analogue cables from the cavern
    - Hard to remove from cavern cable trays?
- Install new RODs and L0Calo/L1Calo in USA15
  - Mass of new underfloor fibres
  - Lay new fibres from detectors to RODs
- Test complete chain: FE via RODs to L0Calo & ROS
  - Known test patterns useful (as well as calibration signals)
- No time to debug USA15 ROD/L0Calo/ROS system
  - Need to have a full scale test outside USA15 beforehand
    - Request 15 or 20 rack test rig the year before installation?
  - Use limited installation time for what cannot be tested earlier

Fallback (Please Not!)

- A very unwelcome fallback option has been discussed if the Calo FE and RODs are replaced soon but new L0Calo cannot be built on the same timescale
  - Build system to convert data on fibres from new RODs to LVDS electrical signals expected by existing L1Calo CP/JEP
    - Needs all final optical components, many FPGAs, four ATCA crates?
    - Still quite expensive, would be replaced soon, no trigger improvement
    - Really, really hope we would not need to do this!

Existing system



Fallback: new Calo FE and RODs, old L1Calo

Work Done

- Exploring phase 2 architecture ideas
  - With no guidance from simulation yet
- Interaction with LAr/Tile on interface with LOCalo
  - Layout of FE links to RODs
- Topological processor studies
  - Simulation, algorithm and architecture
    - Aimed at phase 1, a lot can be carried over to phase 2

To Be Done

- Simulation, simulation, simulation!
- Present simulation work has concentrated on phase 1
- Need to seriously start studying phase 2
  - Look at how (or whether) finer granularity can help
  - What is the best way to use it
    - Formation of "mini towers"
    - Algorithms from L2 or other ideas
  - Use of L1Track in combination with L1Calo/L1Muon
    - Work has started on the L1Track side
  - Large program of work not really started