"L1Calo" Upgrade Phase 2

Murrough Landon
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- Introduction
- Granularity and algorithms
- RODs, links and mappings
- L0Calo/L1Calo design?
- Summary

Introduction/Reminder

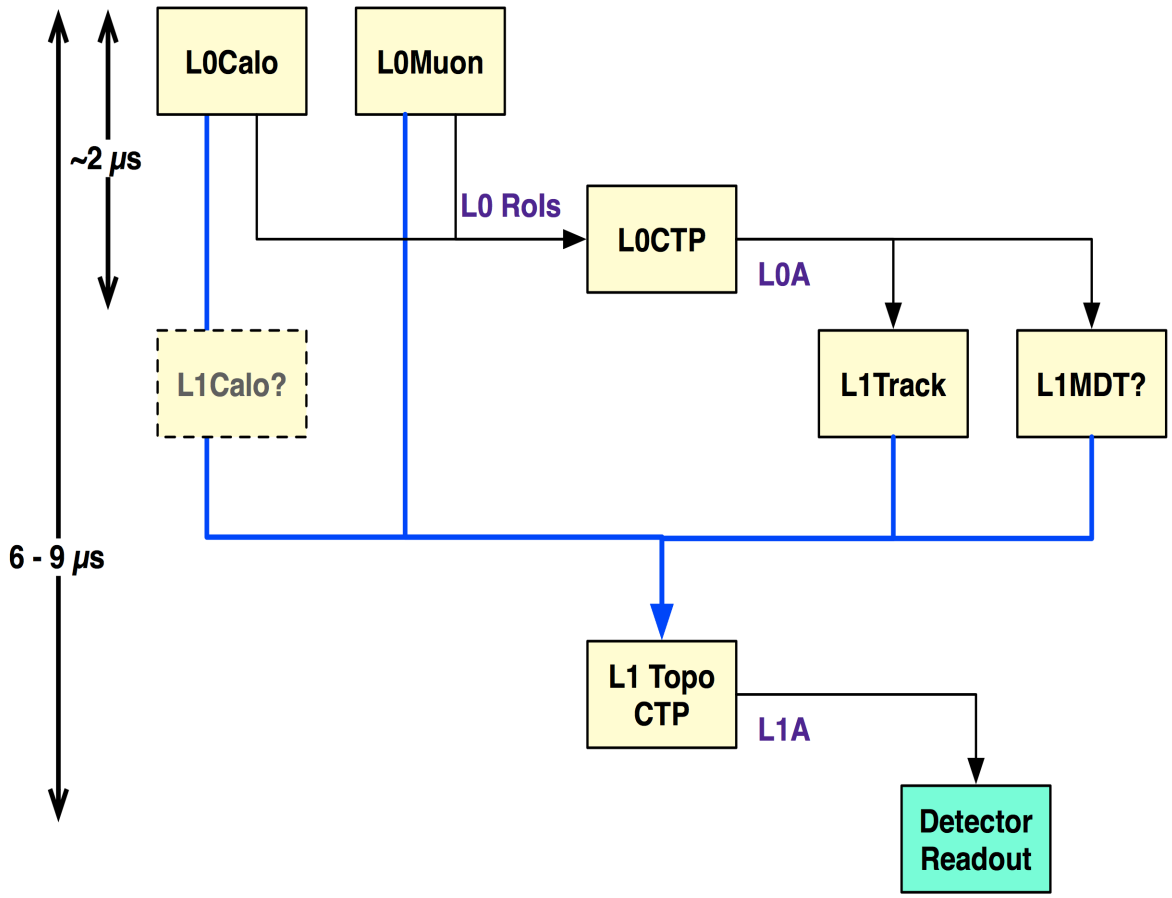
- LHC phase 2 luminosity upgrade expected ~2020?
  - Aiming to reach about 5*10^34, but no increase in energy
    - Recent suggestion that Calo readout upgrade may be earlier?
- Trigger requirements
  - Still interested in the same objects (W,Z,etc)
  - Hope to keep thresholds as close to 10^34 menu as possible
  - But the interaction rate and pileup is much higher
  - So we will need a significantly more discriminating trigger
    - Over 99% of "phase 0" L1Calo electron triggers are jets
  - Use much finer granularity information from the calorimeters
    - Mainly from the EM layer

L1Calo Upgrade Work

- Mostly concentrating on phase 1 upgrade
  - Expected to be required by ~2015?
  - Topological processor architecture proposed
  - Several people working on simulation
    - Scenario already looks much worse than expected in the TDR
  - Various demonstrator boards being designed
    - Both small scale standalone and ATCA based modules
- Still rather little done towards phase 2
  - Looked at algorithms to steal from current Level2
  - Some thought on interface with RODs
  - Rough ideas on overall architecture and bandwidths
  - No attempt at simulation yet

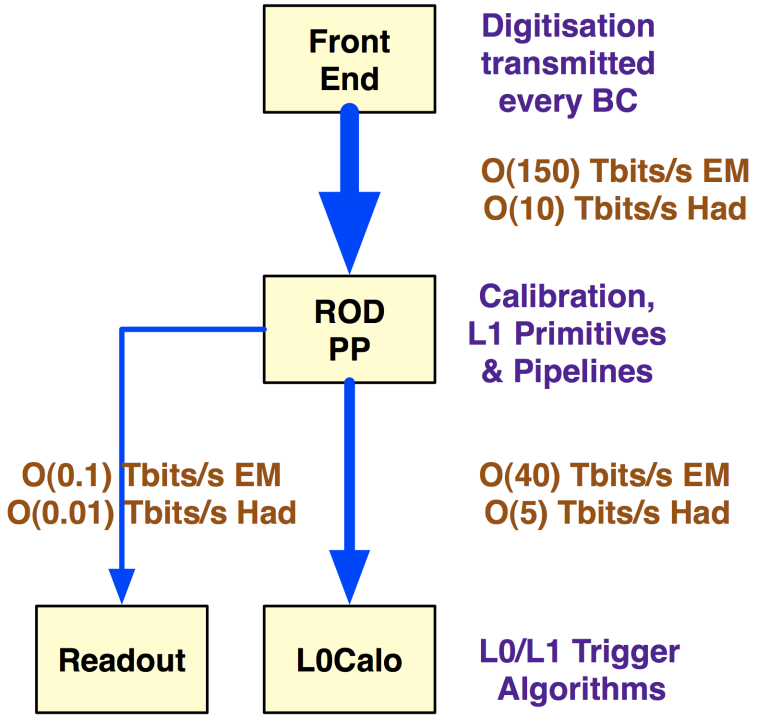
Likely Phase2 Trigger

- Fast Level0 Calo and Muon RoIs
  - For L1 track trigger(s)
  - Up to 500 kHz of L0As
- Slower Level1 topological trigger
  - Using a combination of calo, muon, inner tracker (and MDTs?)
  - May also have L1Calo refinement of original L0Calo trigger?
  - < 100 kHz of L1As?



Calo Front End, ROD and L0Calo Links

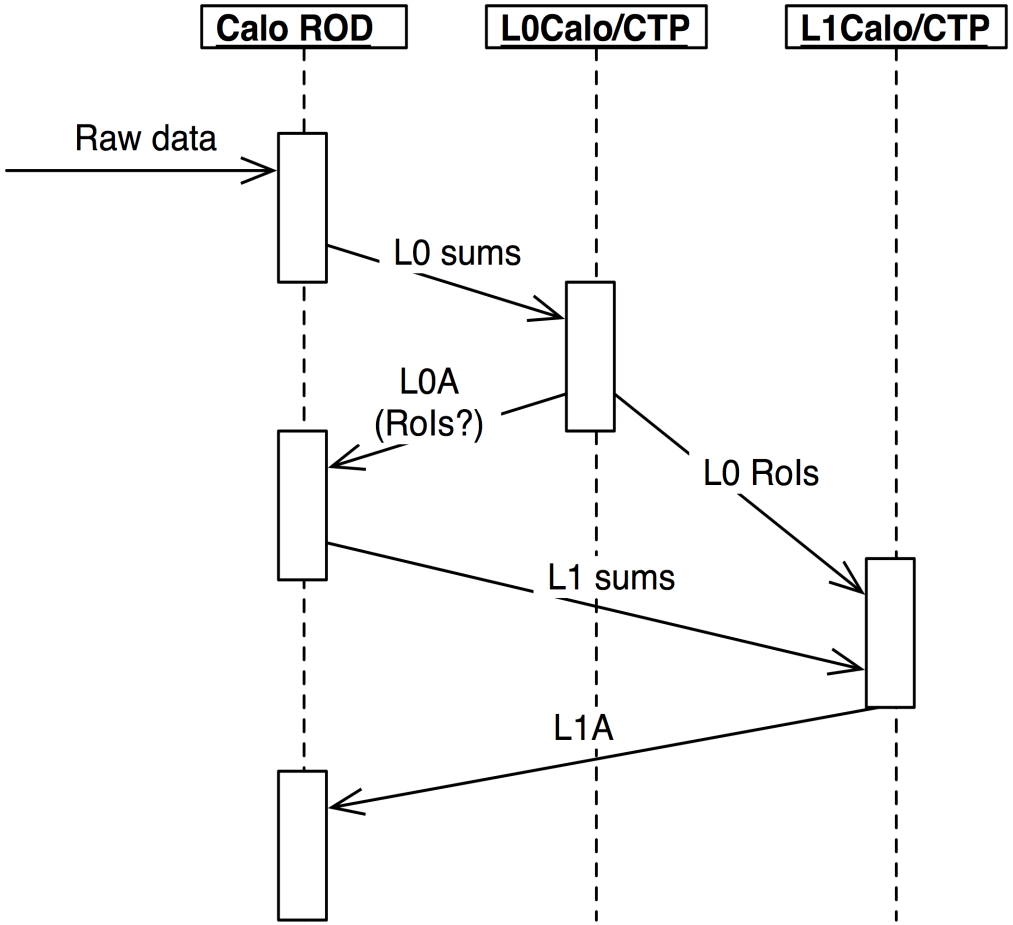
- Digitise all cells every BC and transmit to RODs in USA15
- Preprocess for L1Calo
  - Et assigned per BC
  - Maybe also precise timing?
  - Fine granularity sums
  - Location within mini towers?
    - Coordinate of EM strip max?
  - Quality flags
    - Pile up detected
    - Fine structure in EM strips?
      - Eg for π0 rejection



*NB bandwidths are **very** approximate!*

Possible Additional L1Calo Stage?

- Suggestion to use the L1 stage also for refining the L0Calo decision
  - Mainly for EM layer (strips)
  - But could (re)process full calo data at 500 kHz
- Adds complexity to the calorimeter RODs as well as the trigger
  - Use RoIs? Or just L0A?
- Need a good idea of how it would be used



Granularity

- Present L1Calo
  - Mainly based on 0.1*0.1 towers in both EM and hadronic
  - This is the hadronic layer detector granularity
  - But EM layer has much finer granularity – underused so far
- L1Calo Phase 2
  - Not much change in hadronic layer?
    - Would more depth samplings be useful?
    - Might anyway be worth separating Tile D cells (0.2*0.1 geometry)
  - Expect big (tenfold?) increase in EM data to phase 2 L1Calo
    - Need to study what is the most useful information to send
    - Plenty of opportunities for people to work on simulation!

Algorithms

- Basic sliding window with finer granularity (.05*.025?)
- Try to import good algorithms from present L2
- Best EM selection is based on shower shape:
  - Look at ratio of 3*7 vs 7*7 middle layer cells
  - Simulation question: how does this degrade with granularity
    - Suppose we had sums of 2 middle cells (matching back layer cell)
    - Would have to look at 4*7 vs 8*7 cells
- Next best (for π0 rejection):
  - Look for fine structure (double peaks) in strip layer
  - This really needs the full granularity to be useful
    - Probably too much data to ship to L0Calo (could go to L1Calo?)
    - Good candidate for more sophisticated ROD preprocessing?
  - Simulation/algorithm/firmware question: what would be the best way to process and transmit this information?

Links to L0/L1Calo (1)

- EM layer:
  - Suggest one 10 Gb/s fibre per 0.1*0.1 tower (all layers)
    - Allows about 200 bits of payload data per BC (might like more!)
  - Example allocation of bits (all depth samplings separate)
    - Keep phi granularity (middle/back), sum to 0.05 in eta
    - Eight 10 bit (Et+quality?) back layer values [80]
    - Eight 10 bit middle layer sums plus max cell bit [88]
    - Two 10 bit strip layer sums plus 8 coordinate/quality bits [36]
    - Two 10 bit PS layer sums plus 1 coordinate bit [22]
    - Total 226 bits (and we would like some spare bits too)
  - Maybe additional 1 fibre with low granularity (0.1*0.1) sums
    - Useful if jet/energy trigger is in a separate FPGA or module
  - Additional fibres per 0.4*0.2 with extra info for L1 stage?
    - Full strip layer information for π0 rejection and track matching?
    - Precise timing for z vertex and/or slow heavy exotic particles?

Links to L0/L1Calo (2)

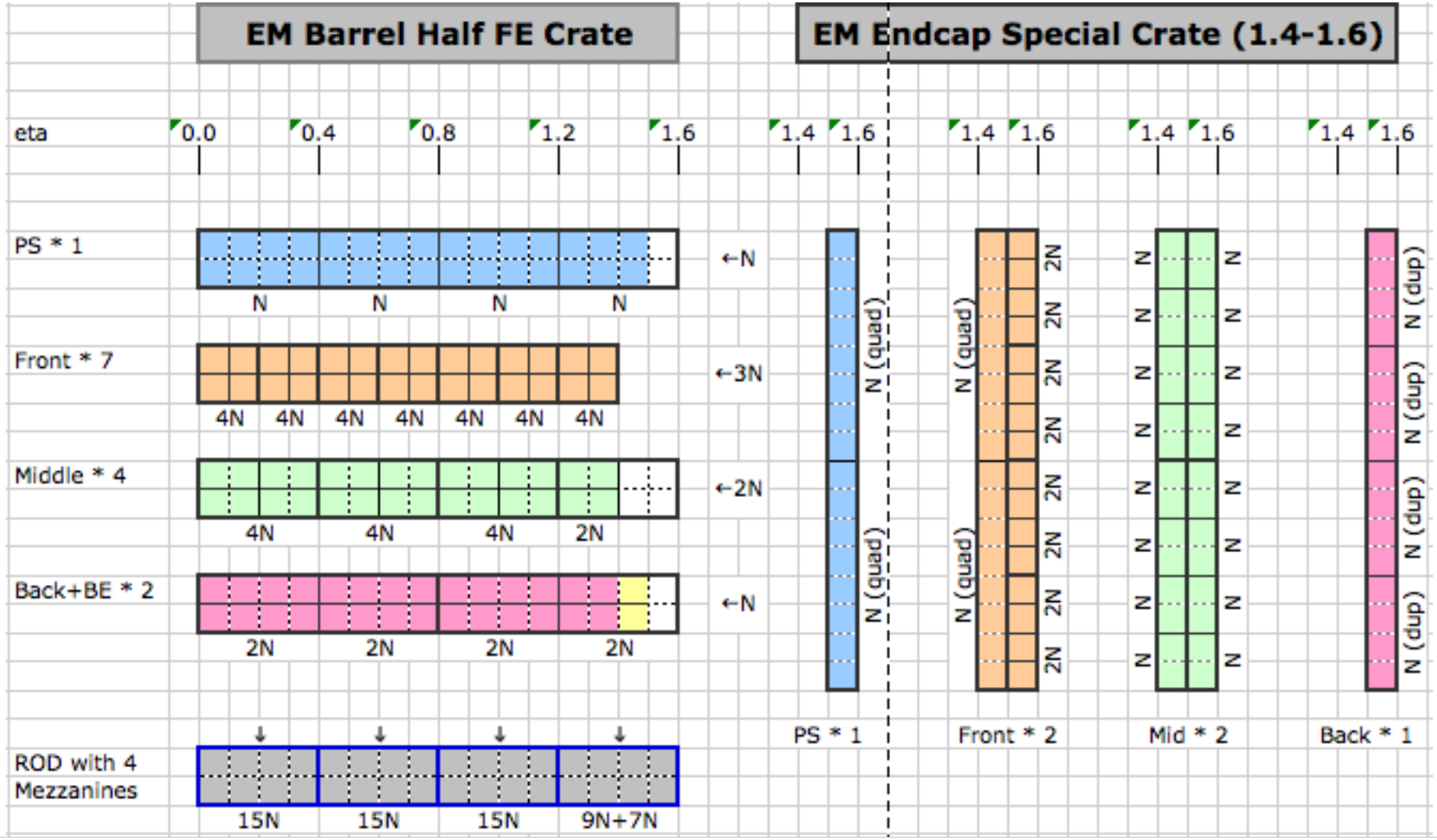
- Hadronic layer:
  - Suggest one 10 Gb/s fibre per eight 0.1*0.1 towers
  - Allows about 25 bits per tower
    - Energy plus some depth profile (separate D layer?) and quality bits?
  - Good to (slightly) underuse the bandwidth
    - Need to cope with extra cells in overlap regions
    - Eg crack and gap scintillators
    - Tile and HEC cells in 1.4 to 1.6 region
    - Might have up to ten towers per link in places
- More compact in low granularity endcaps/FCAL?

LAr and Tile RODs

- LAr
  - Latest aim is for one ROD to cover one half FE crate
    - Or same number (1800) of cells with different eta*phi shape
    - ROD would contain four TCA mezzanines (with 1 FPGA?)
  - L1Calo (my!) preference
    - One EM ROD mezzanine covers a "domino" of 0.4*0.2 (eta*phi)
      - Larger area in the high eta EM endcap region, HEC and FCAL
    - Aim to keep the shape the same across the eta phi space
      - Easier for fanout – but harder in standard EM Endcap region
- Tile
  - Current Tile proposal: ROD covers 3.2*0.1 in eta*phi
    - Much less dense than LAr ROD: could be more ambitious!?
  - L1Calo (my!) preference:
    - ROD covers 0.2 in phi (either split at eta=0 or more dense)
    - Match the EM 0.4*0.2 domino when grouping towers on links

LAr EM Barrel/Overlap Mapping

- Attempt to map links from front end boards (FEBs)
  - Tricky regions need duplication/quadruplication of fibres



ROD Outputs to L0/L1Calo?

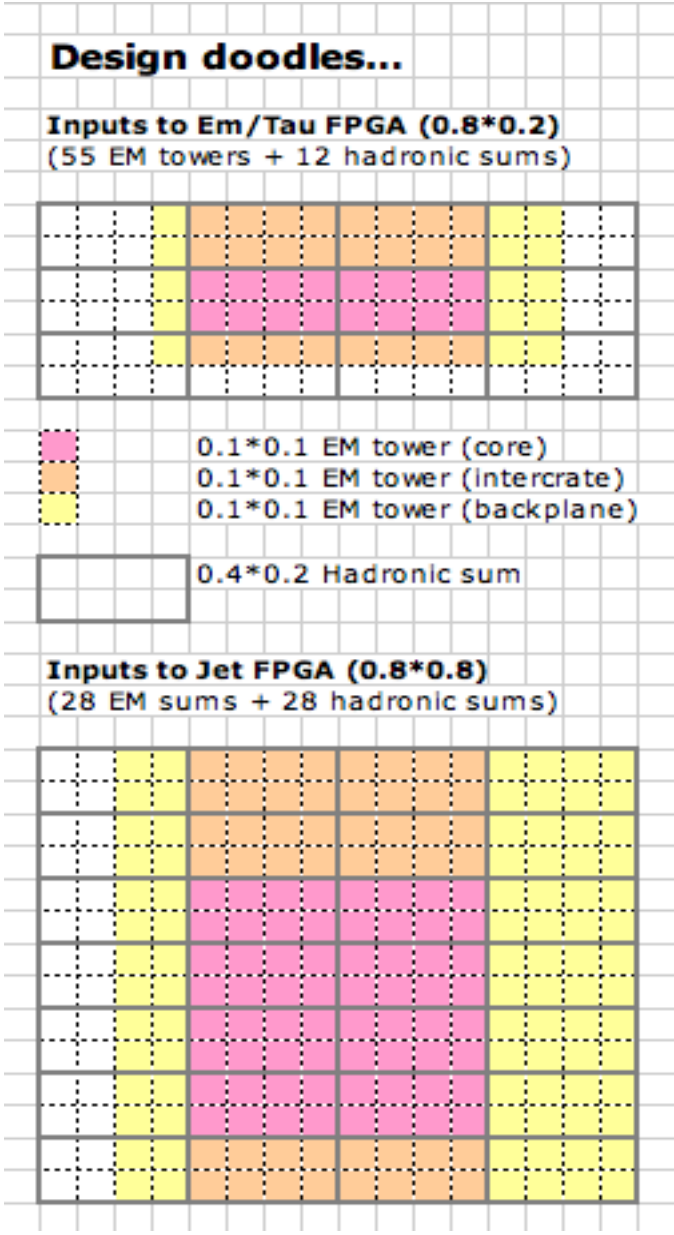
- EM layer
  - Probably four 10 Gb/s SNAP12 bundles per ROD
    - One per mezzanine (less if higher speed links which is likely)
    - Same for all eta, but RODs & links somewhat underused at high eta?
- Hadronic layer (HEC and Tile)
  - Depends on density of channels per ROD
  - HEC/FCAL RODs likely to be (half?) as dense as EM RODs
  - For present Tile ROD, ~half a SNAP12 bundle per ROD?

Inputs to L0/L1Calo

- One 0.4*0.2 area in eta*phi might have:
  - 8 EM fibres covering one 0.1*0.1 tower each
  - 1 Hadronic fibre covering eight 0.1*0.1 towers
  - Perhaps additional 1 EM fibre with low granularity sums
    - Useful if Jet/Energy algorithms are in a separate FPGA
    - NB such low granularity sums are the main constraint on organisation of cells into RODs (both for LAr and Tile)
  - And maybe additional fibre(s) per 0.4*0.2 area with extra information used only by L1 trigger (not for L0)
  - Above still assuming 10 Gbit/s links
- Regroup to one SNAP12 with EM+Had fibres
- Optically duplicate each bundle at the same time
  - Intercrate fanout
  - Electrical fanout within crates (no de/reserialisation)

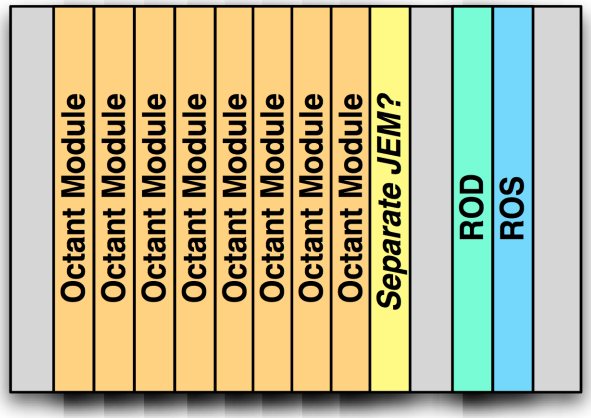
LOCalo Phase 2 Architecture? (1)

- Single processor module (0.8*0.8)
  - For all objects: EM, tau, jet
  - Perhaps four big FPGAs per board?
  - If so, could have one FPGA per 0.8*0.2
    - If we have one fibre per 0.1*0.1 tower:
    - 11*5 EM fibres plus 4*3 hadronic fibres
    - Separate FPGA (one per module) for jets?
      - Unless future FPGA handles lots more inputs?
    - Total of 88 0.1*0.1 fibres plus 2*28 0.4*0.2 sum fibres per module
    - Around 12 SNAP12 fibre bundles
    - About 1.5 Tbit/s total bandwidth per module
- Or could imagine separate JEM
  - One per octant crate covering all eta
    - Same module, different firmware?

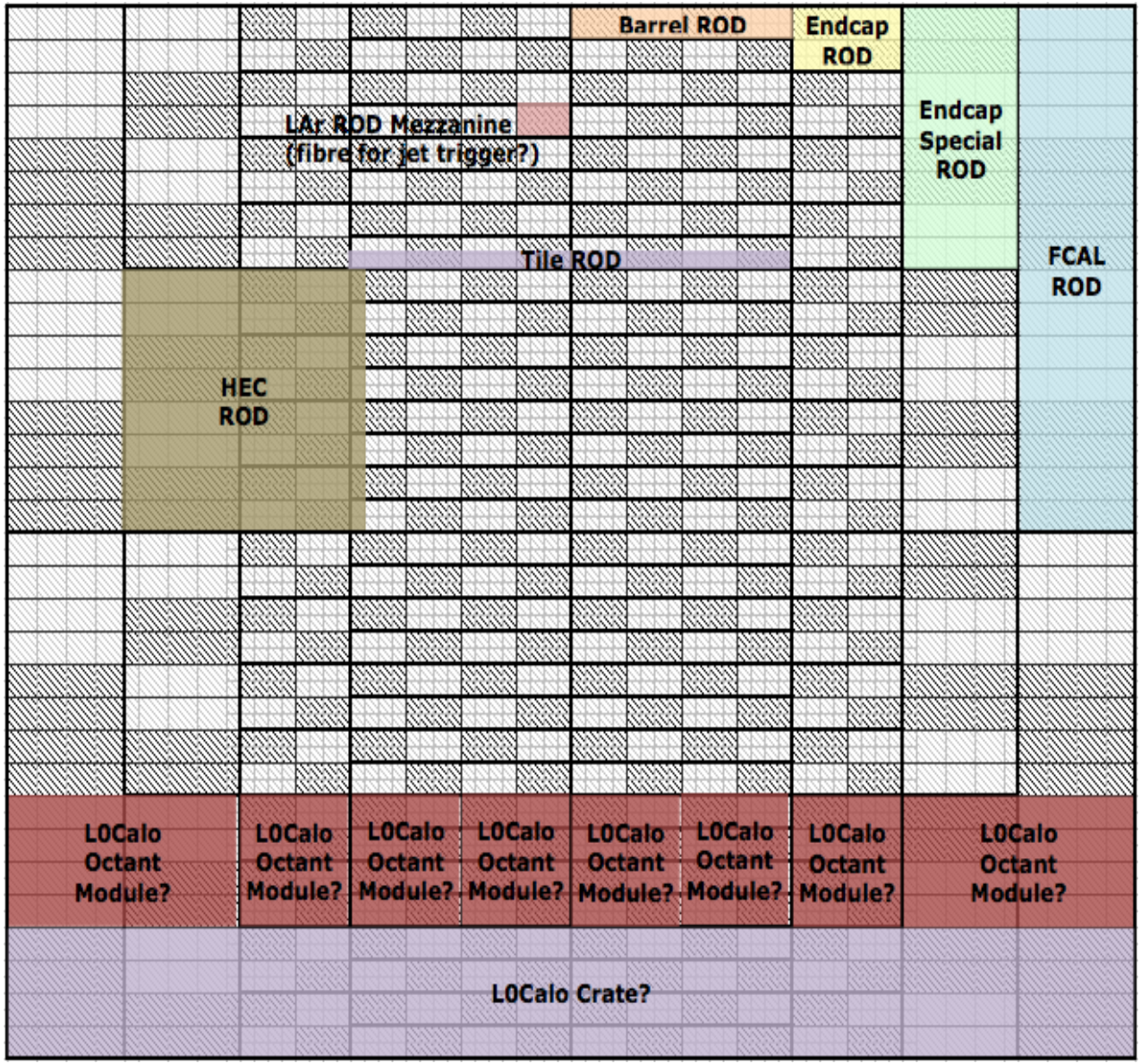


L0Calo Phase 2 Architecture? (2)

- Phi octant layout
  - Intercrate fanout from RODs, eta fanout via backplane
  - Output to global topological merger
  - ROD/ROS in same crates?



L1Calo ATCA crate? (One octant, all eta)



Summary

- Trying to get a rough L0/L1Calo design
  - Are our current thoughts reasonable?
- L1Calo/LAr/Tile working group started discussions
  - Organisation of RODs and links, bandwidth, etc
    - How to match up LAr/Tile, barrel/endcap layouts in manageable way
    - Is denser Tile ROD or half eta slice possible? (If required?)
  - Granularity of L0/L1 sums and content of data
  - Any other preprocessing we would like
  - Implication of new ideas for L1Calo stage
    - Extra data from ROD following L0A (full granularity and/or RoI based)
- Prototyping and technology demonstrators under way
  - Mainly aimed at phase 1
- Important to get input from simulation!