Phase2: Calo FE and L1Calo

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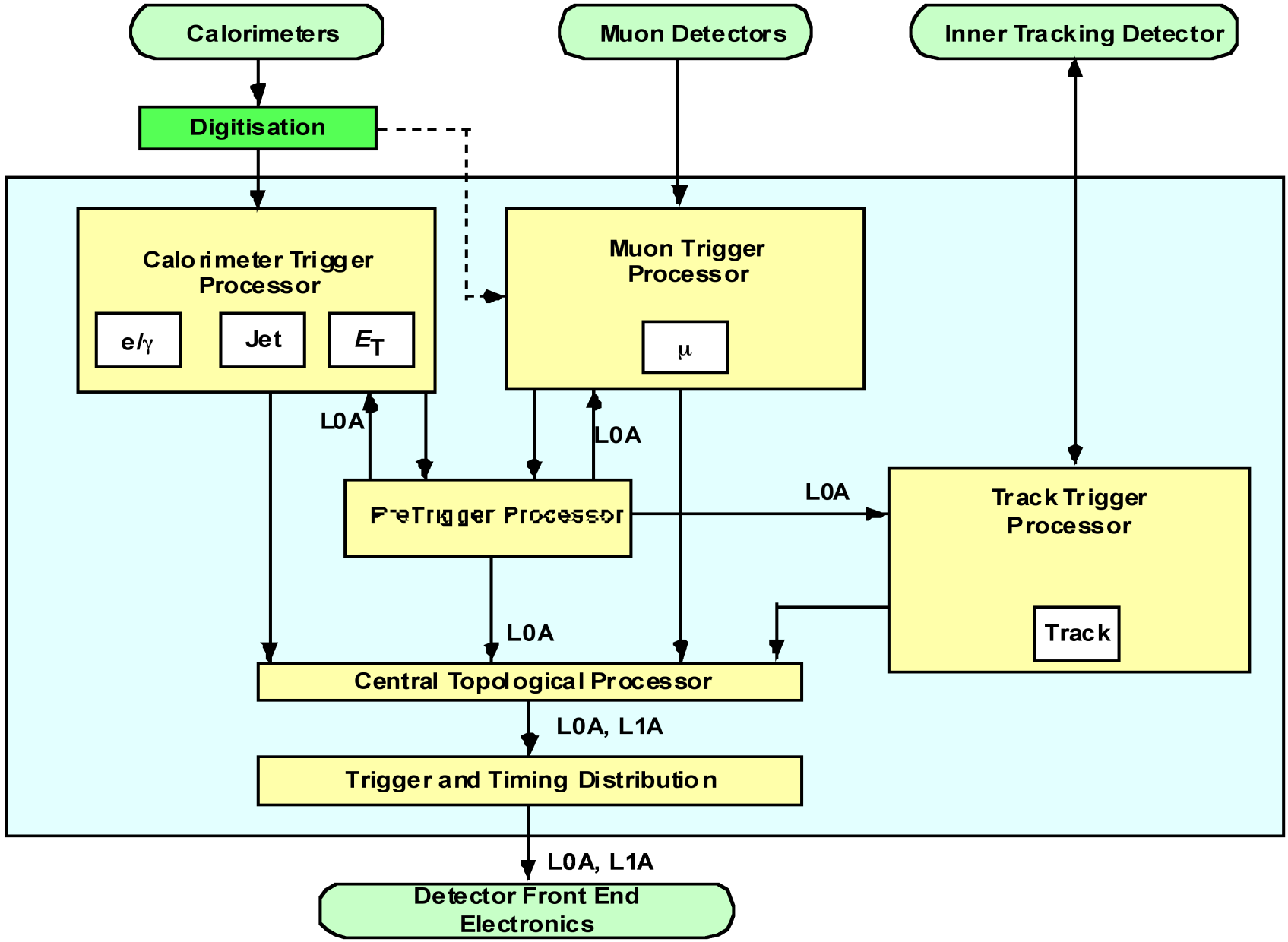
- Phase 2 Overview: L0 and L1
- LAr and Tile plans
- Possible L0Calo system
  - Links, algorithms, architecture
- (No simulation)

Overview of Phase 2

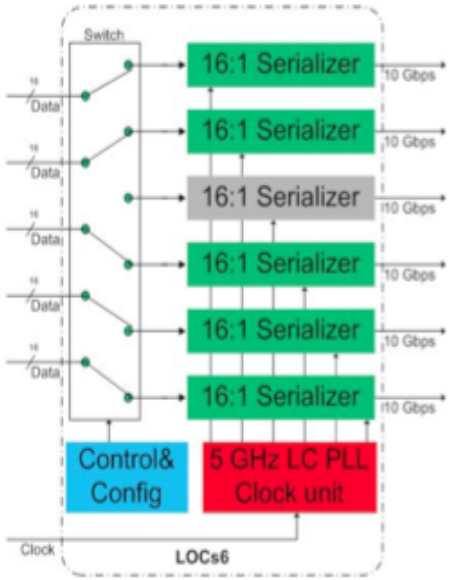
- Present L1A split into L0A and L1A
  - To allow L0 RoI seeded L1 track trigger
  - L0A: synchronous, low latency (3μs), rate up to 500 kHz
  - L1A: asynchronous within fixed longer latency (≥9.6μs?)
- Calorimeters: move pipelines off detector
  - Digitise every cell every BC and send to ROD
- Calo RODs preprocess "minitowers" for new "L1Calo"
  - New "L1Calo" comprises L0 and L1 trigger processors
- L0 and L1 topological processors
  - Including muon and (at L1) track triggers
- NB terminology is unsettled
  - L0 ≈ "pretrigger", word "L1Calo" is overloaded etc

Overview of Phase 2



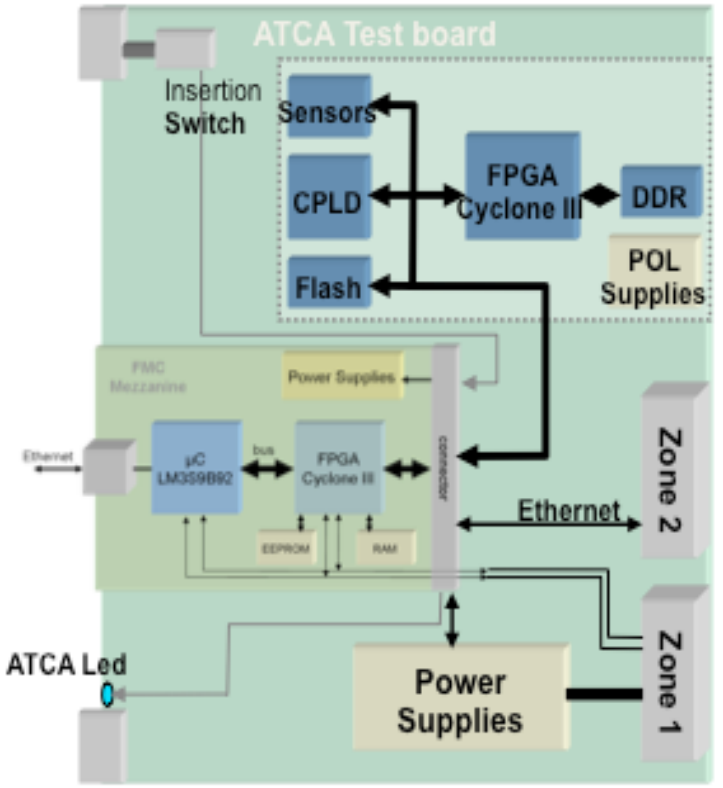
LAr Upgrade Plans (1)

- Front End
  - No change to cabling from calorimeter to FE crates
  - New Front End Board (FEB)
    - Digitise every channel every BC and send to ROD
    - Requires rad hard ADC and fast serial links
    - Baseline: one 10 Gb/s SNAP12 per FEB (128 channels)
      - Organised as two sets of 64 channels on five fibres with one redundant fibre
  - Active R&D programme
    - COTS ADCs tested: none OK (power, price, rad hard)
    - Custom ADC being developed: early version promising
    - Custom serial link being developed
      - Single channel version tested (incl radiation hardness)
      - Six channel version being designed



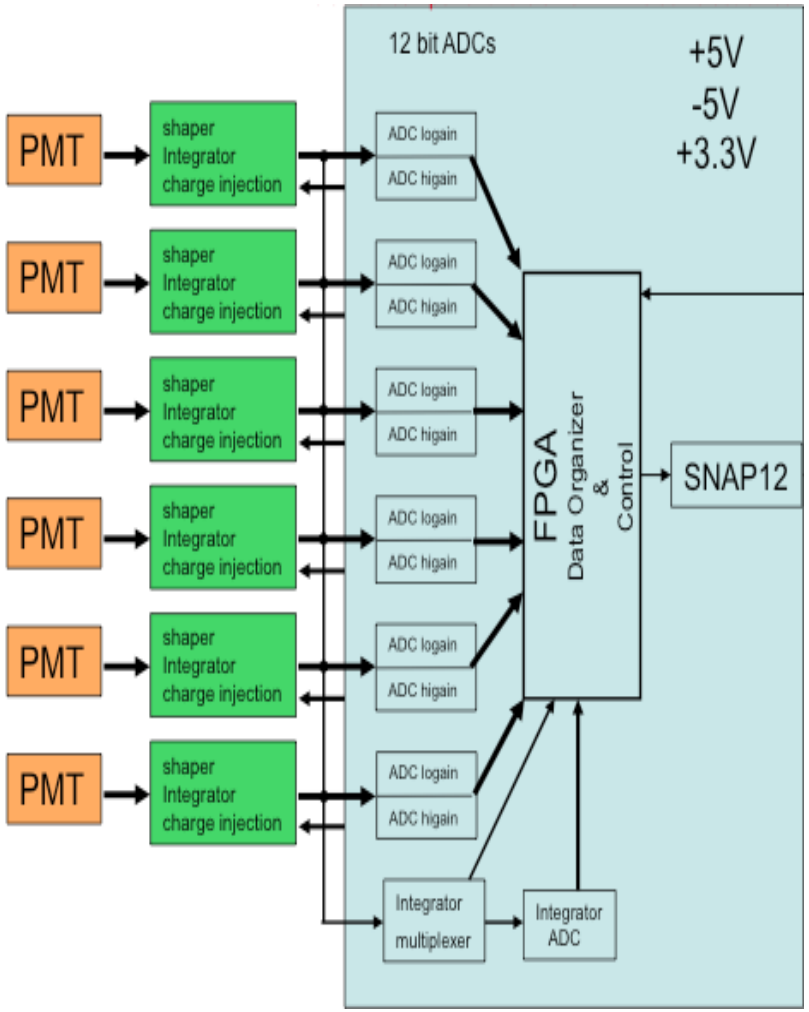
LAr Upgrade Plans (2)

- ROD
  - Baseline: ROD per half FE crate (14 FEBs)
    - 14 SNAP12s, input bandwidth 1.4 Tb/s
    - Expect about 400 Gb/s output to L0Calo
  - Full system needs O(100) such RODs
  - R&D programme:
    - Prototype ATCA test module produced
      - ATCA mezzanine being assembled
    - ROD evaluator board being designed
    - ROD firmware: tested optimal filter & BCID for one channel
    - Estimate of latency
- Other
  - Power supplies, etc



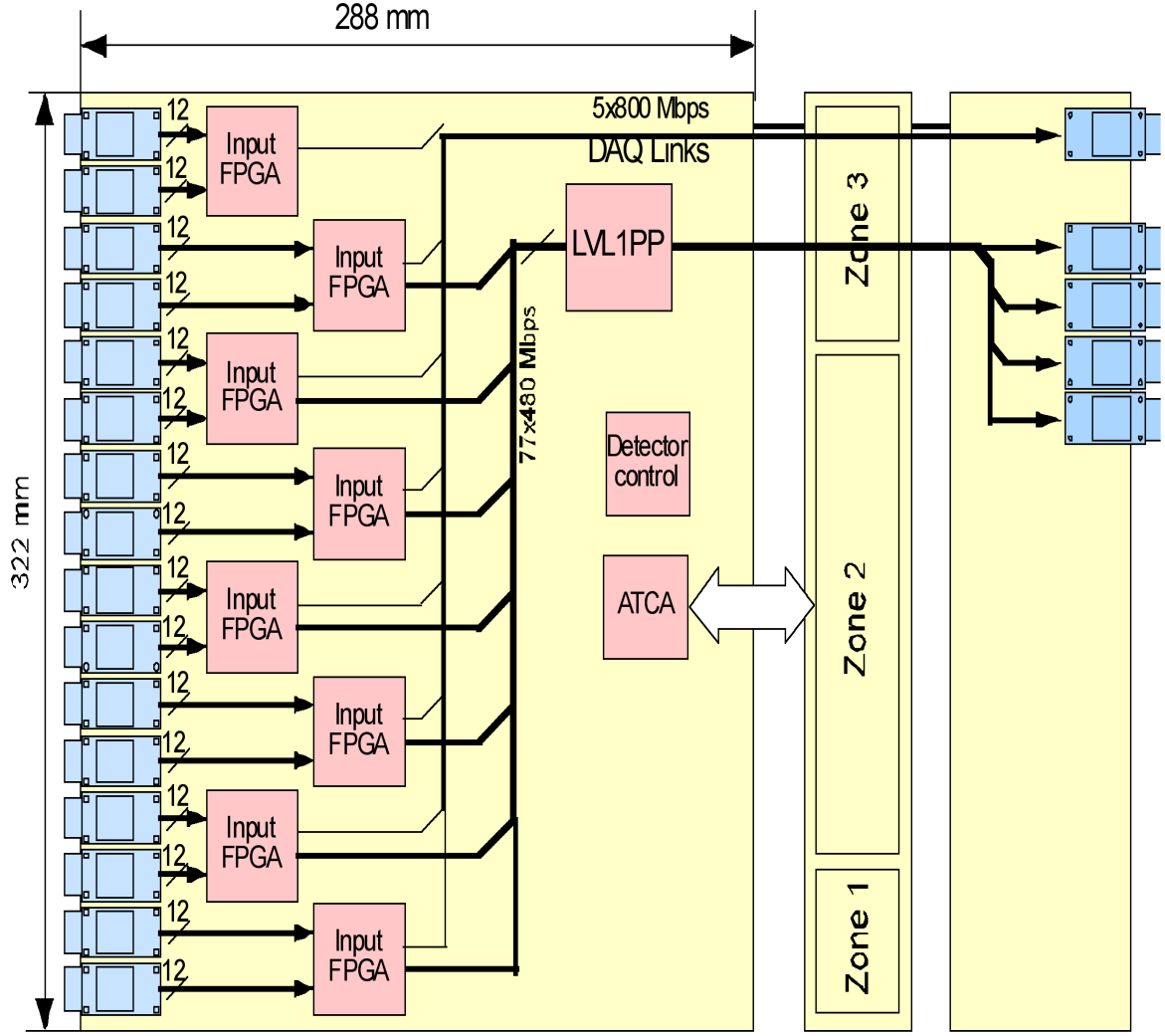
Tile Upgrade Plans (1)

- Front End
  - No changes to the detector
    - Except drawer mechanics
  - New drawer electronics
    - Digitise every channel every BC
    - Expect to use commercial ADC and CERN GBT links
    - Baseline: one 5 Gb/s SNAP12 per drawer (up to 48 channels)
      - Fully redundant readout, every PMT independently transmitted twice
  - R&D work
    - New FE components under test
      - New ASIC for "3 in 1" function
      - PMT block



Tile Upgrade Plans (2)

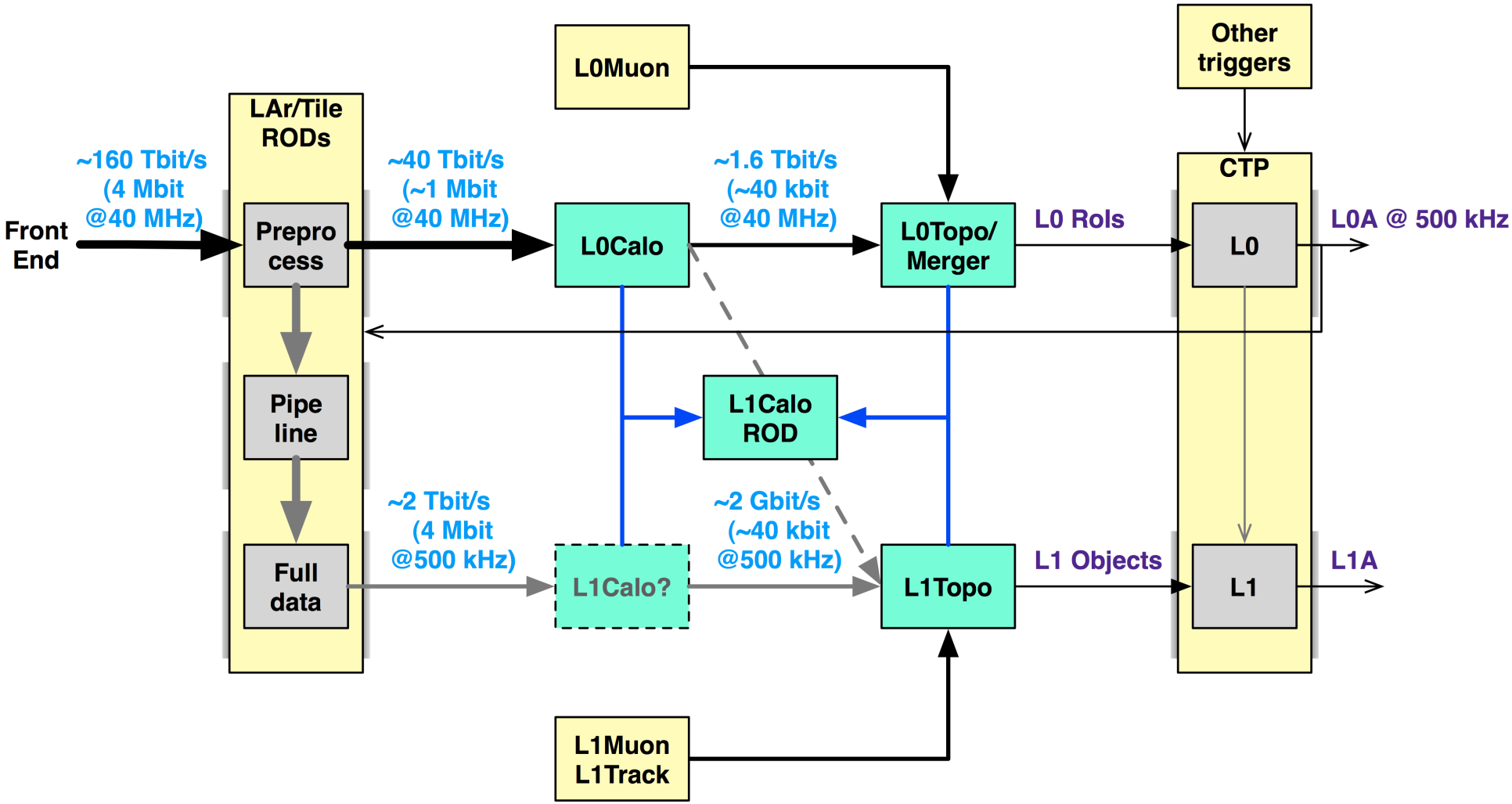
- ROD
  - Baseline: one ROD per eta slice (EBC-LBC-LBA-EBA) * 0.1 phi
    - NB 0.2 phi and half eta preferred by L1Calo
    - Expect about 40 Gb/s output to L0Calo
  - Needs 64 such RODs
  - Tested GBT links
  - No latency estimate yet
- Other
  - Drawer mechanics
  - Power supplies



Calo ROD – L0Calo Interface

- Calorimeter ROD functions for L0Calo:
  - Derive calibrated Et from digitised pulses (no saturation)
  - Assign Et to correct bunch crossing
  - Provide quality flags from optimal filter (pile up, etc)
  - Form sums of calorimeters cells into "mini towers"
    - Definition of mini towers (or "L0 primitives") to be defined
    - EM layer: both fine and coarse sums (for EM & Jet triggers)
  - Possibly run algorithms on cells within one ROD FPGA
    - Eg π0 rejection using LAr EM strips
  - Transmit mini towers to L0Calo
  - Organisation of towers in RODs to be optimised for L0Calo
    - Aim to handle boundary areas and keep flexibility for mini tower formation
  - Pipeline full data (for every cell) for use by L1 stage (& DAQ)

Baseline Phase 2 L1Calo Architecture

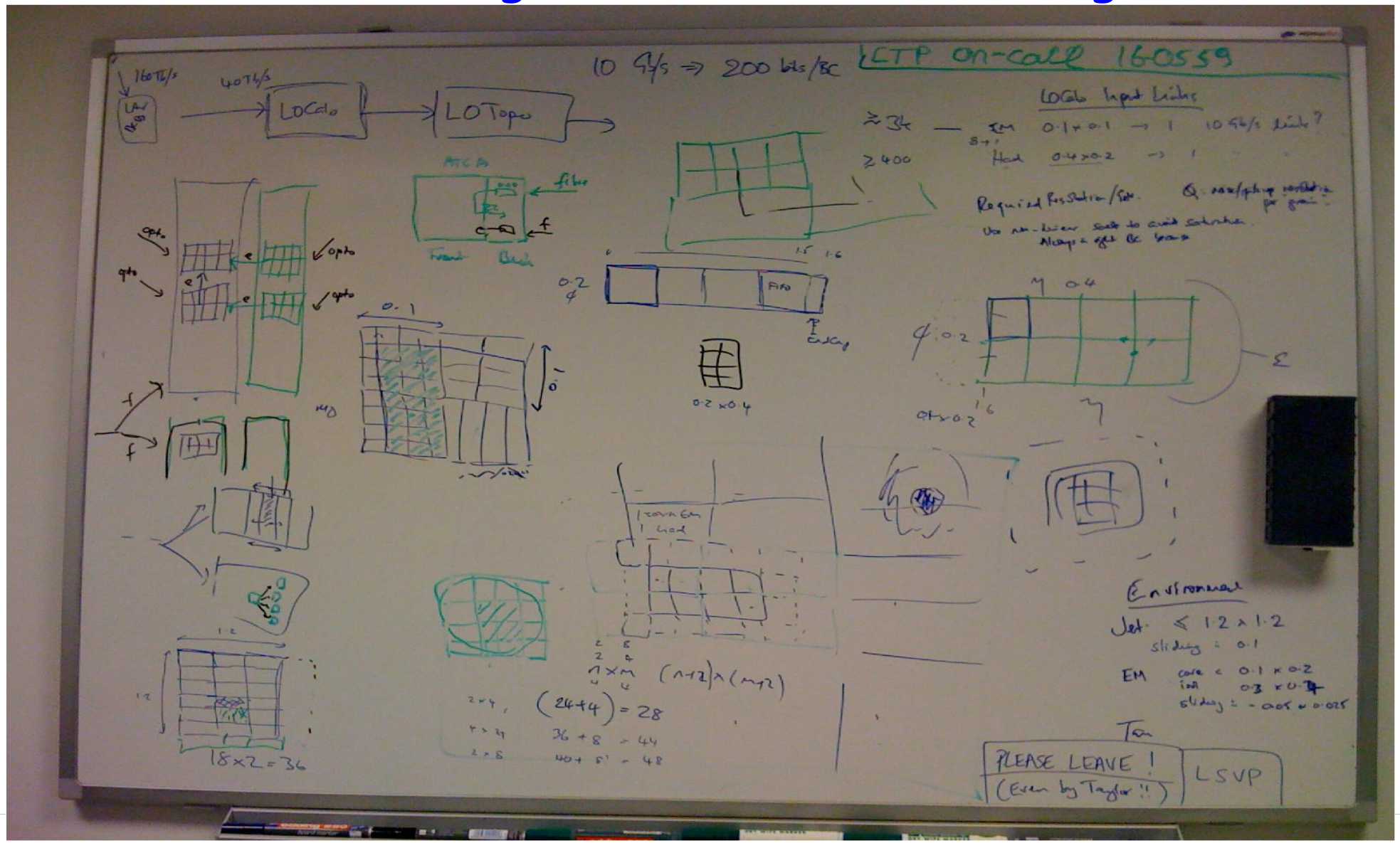


Phase 2 L1Calo Components

- L0Calo:
  - Find EM, Tau, Jet objects (and Et sums) every BC
  - Large multi module system
- L0Topo:
  - Topological processor: merge L0Calo & L0Muon results
- L1Calo:
  - Asynchronous refinement of L0Calo using full calo data
    - May be driven by L0 RoI (but not necessarily so)
- L1Topo:
  - Final topological processor for L1Calo, L1Muon & L1Track
- L0 & L1 CTP:
  - Interface with topological processors to be defined

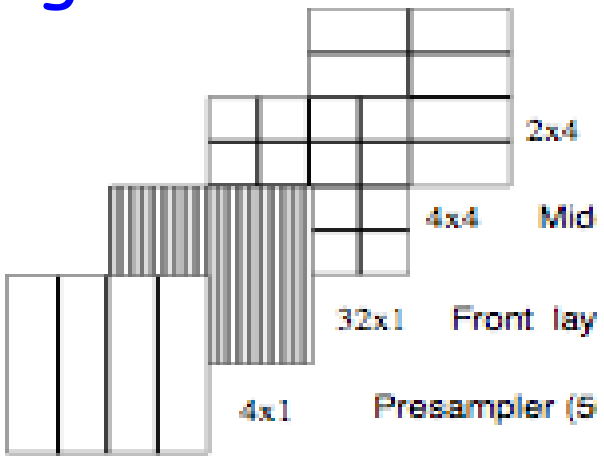
LOCalo Component: Brainstorming

- Discussed existing ideas, also with our engineers



Calo ROD – L0Calo Links

- Baseline: 10 Gb/s links => 200 bits per bunch crossing
- Hadronic layer (and coarse EM sums for jet trigger):
  - One 10 Gb/s fibre link per 0.4*0.2 (or 0.2*0.4) in eta*phi
    - Can have finer eta*phi and depth granularity than now for jets
- EM layer fine granularity for EM/Tau algorithms:
  - One 10 Gb/s fibre link per 0.1*0.1 tower
    - 200 bits: more detail on eta, phi and depth
    - Concentrate bandwidth on middle layer?
      - Heavily sum strips layer
    - Finer Et resolution and dynamic range
    - Quality bits: pileup flag, strips layer structure bits?

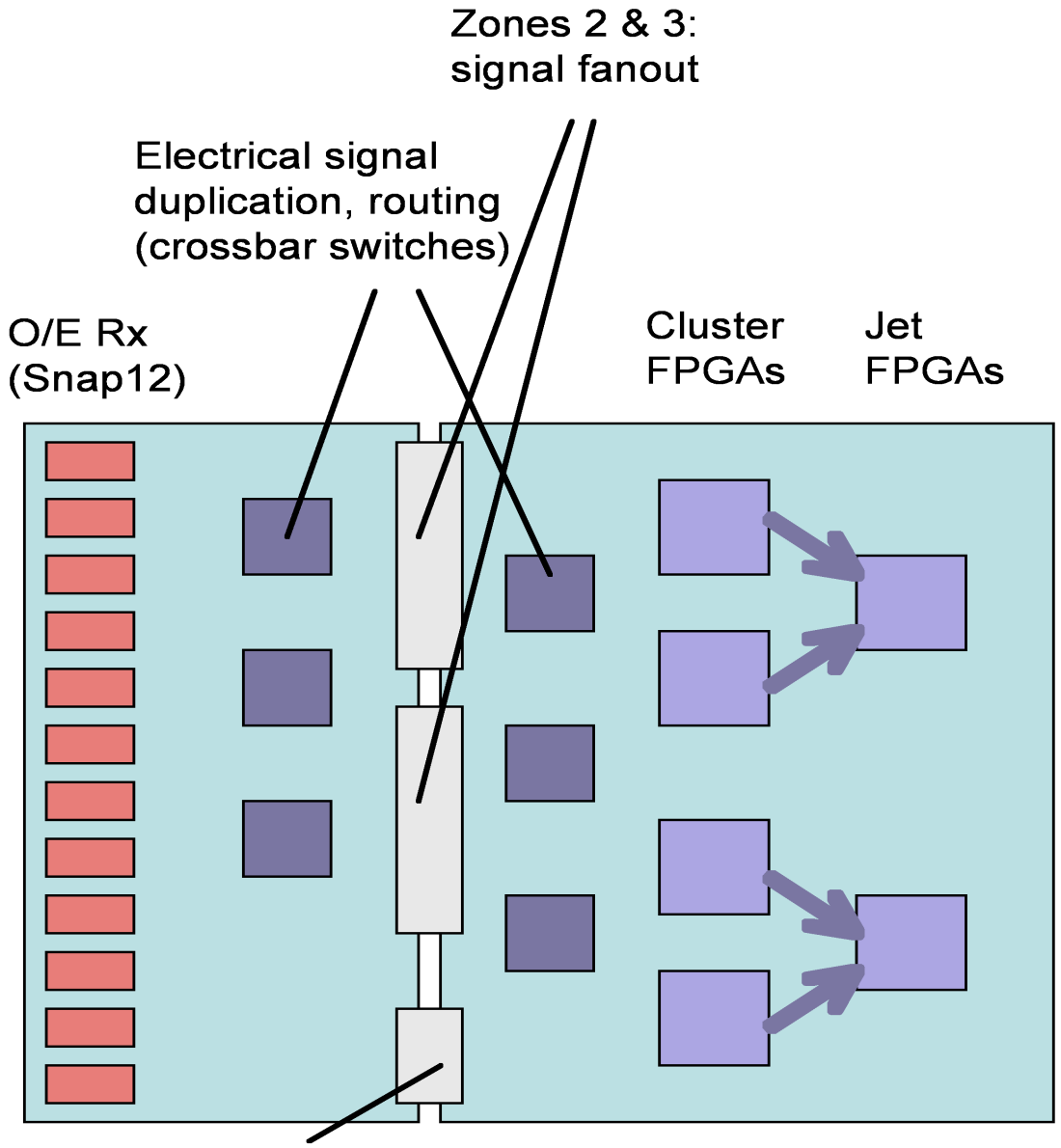


Phase 2 LOCalo Algorithms

- Sliding windows, now with finer granularity
  - Limitations will be fanout and number of inputs per FPGA
    - Expect O(50) 10 Gb/s links into Virtex 7
- Adopt L2 EM/Tau ideas
  - L2 "R core": ratio of 3*7 to 7*7 LAr middle layer cells
    - LOCalo bandwidth might require middle layer cells summed in pairs
    - Need simulation studies on best use of the bandwidth
- Would like larger jet environment...
  - Present 0.8*0.8 eta*phi jets use 0.4*0.4 RoI maximum
    - Better to know if 0.8*0.8 area is a maximum within its environment
    - Problem: much larger fanout and more fibres per FPGA
    - May have to choose one of: better granularity or larger environment
    - Needs some simulation work...

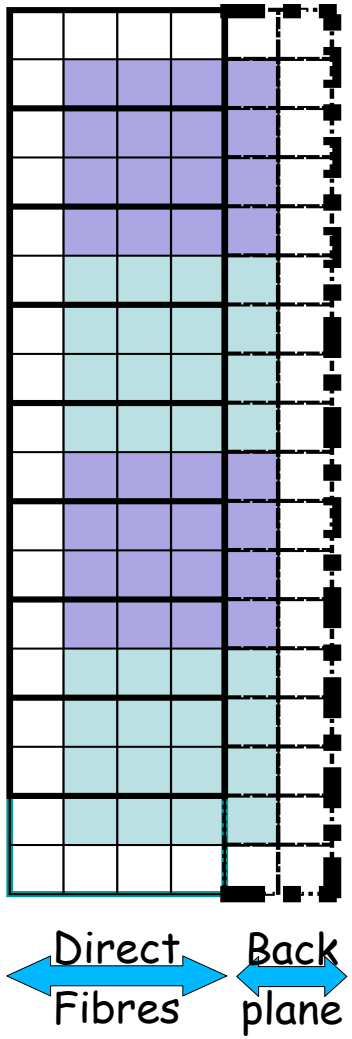
Possible LOCalo Implementation

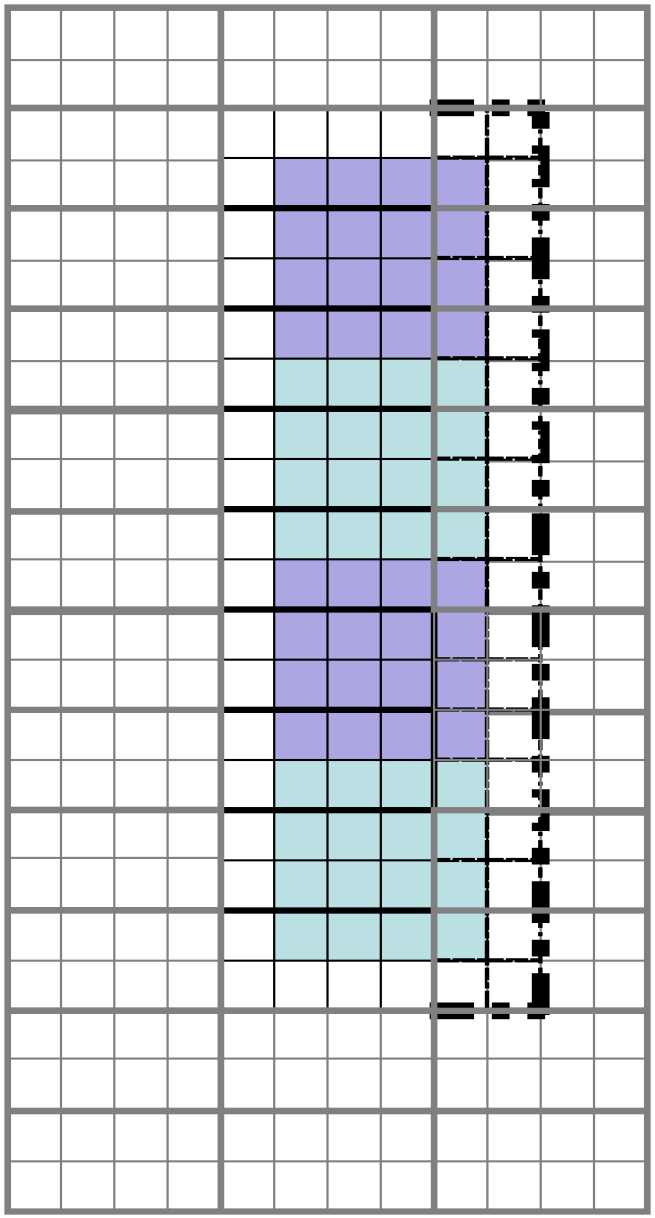
- "Strawman" module
  - Covers 0.4*1.6 eta*phi
  - Both EM/Tau and Jet
    - Resolve overlaps locally
  - Fully custom backplane
    - Fanout to adjacent slots
    - Passive optical fanout for adjacent crates in phi
  - Four full ATCA crates
    - May need >14 slots to handle high eta & FCAL
    - XXL width racks?
    - Or reuse EM/Tau FPGAs in outer modules for FCAL?



LOCalo EM & Jet Fanout

- Need to understand fanout between modules & number of inputs to each FPGA
  - In progress…
    - Not fully worked out yet
  - Examples of EM and Jet FPGAs (0.8*0.8 jets)
    - Coloured areas: one module
  - "Direct" fibres to this module from RODs
  - Environment fanned out from neighbours





Summary

- LAr and Tile progressing well with phase 2 R&D
- L0Calo "straw man" design emerging...
  - Technically feasible (probably)
  - Needs more work on the details
  - Need to define algorithms
  - Estimate latency of L0Calo+L0Topo
- L*EverythingElse: still sketchy or missing
  - L0Topo: use phase 1 topo processor as L0Topo prototype
  - L1Calo/L1Topo: not yet thought about them
- Health warning:
  - Little simulation work to justify these technical ideas