



L1Calo Phase 2 Upgrade

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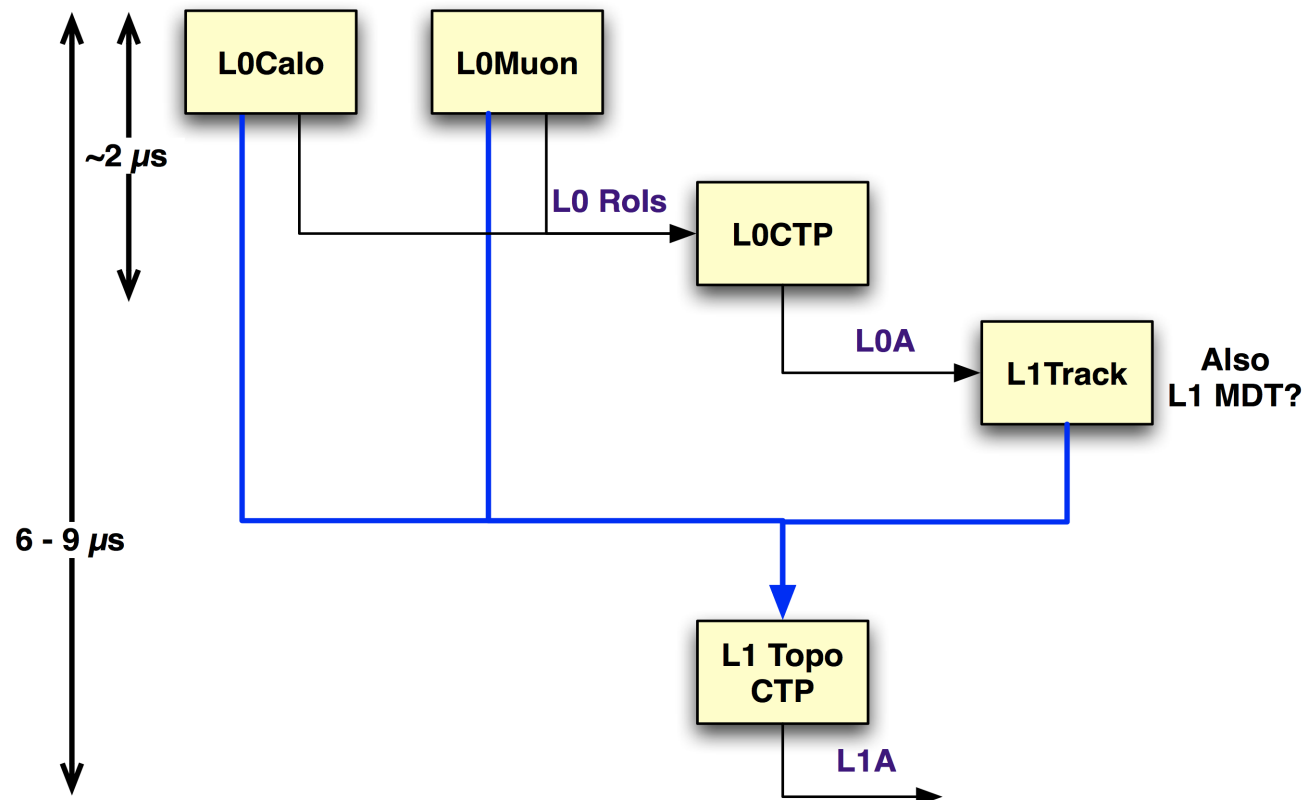
- Recent Progress(?)
- Baseline Concepts
- Design Considerations
- L1Calo Architecture Idea(s)
- Summary

Recent Progress

- Rather little!
 - Main focus of L1Calo upgrade work has been for phase I
 - Simulation is now running (or crawling) at least for 10^{34}
 - Couple of short phone meetings to try to establish who is interested in doing what
 - Needs more follow up
- To be done...
 - Simulation for phase 2
 - Need ATLAS infrastructure and samples
 - Phase 2 work will also need extensive trigger software work to investigate the possible options
 - Detailed thinking about
 - Granularities, algorithms, architectures, bandwidth, technologies

Baseline Phase 2 L1 (and L0) Trigger

- Status of L1Track still undecided?
 - Might still have no L1Track or fully independent L1Track
 - But preferred option is L1Track seeded by “Level0” RoIs
 - This imposes the tightest latency constraint on L0Calo

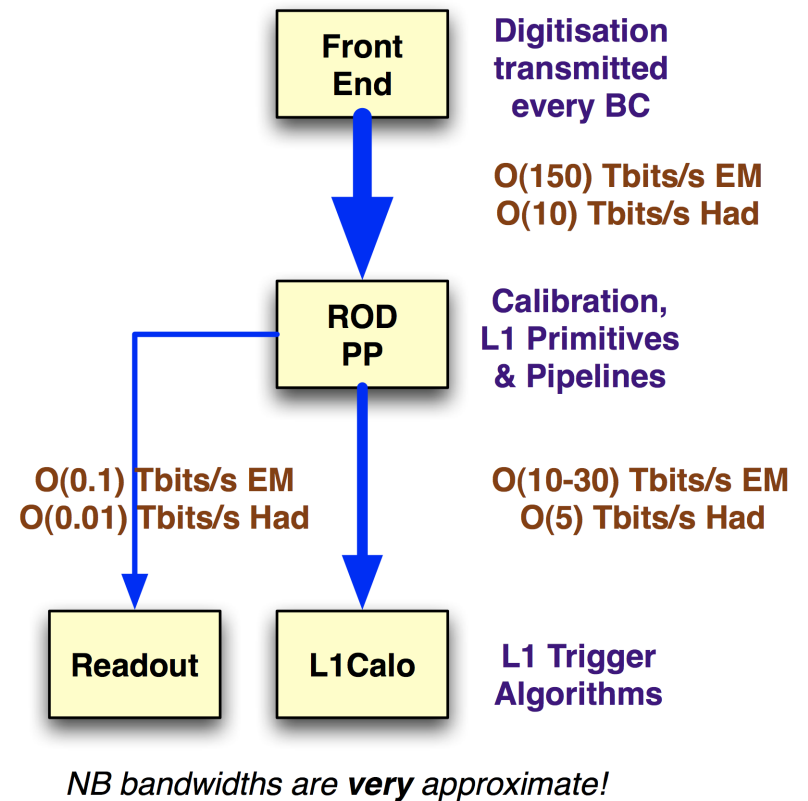


Other Phase 2 L1 Trigger Ideas

- New suggestions, not yet studied:
- Send L0A to all detectors (not just L1Track)
 - Allow muons not to change $3.2\mu\text{s}$ on detector pipelines?
 - L1A acts as fast clear to ROD pipelines
- Two level L1Calo
 - Crude and fast L0Calo (low granularity and bandwidth)
 - Detailed and slower L1Calo (high granularity and bandwidth)

Baseline L1Calo Phase 2 Concept

- **Front end:**
 - Digitise and transmit all cells each BC to off-detector pipelines
- **ROD/preprocessor:**
 - Generate Level 1 primitives (towers++) with calibrated Et assigned to the correct BC
 - Send them to a separate L1Calo trigger processor
- **L1Calo (or really L0Calo):**
 - Run sliding window algorithms over combined EM/Had towers
 - Results to global topological CTP
 - Combining L1Calo/L1Muon/L1Track



Implications of On-Detector Digitisation

- Allows much more sophistication in forming “towers”
 - New digital “L1 Primitive” could be a bit field with
 - Et (to greater precision than before if required)
 - Depth and lateral shower profile information, quality flags?
 - Detailed coordinate from LAr strips layer?
 - Better handling across boundaries?
 - Given suitable mapping of FE to ROD links
 - Finer granularity (in EM layer)
 - Different granularities likely in EM and Hadronic layers
- Single calibration for trigger and main readout
- But brings trigger and readout closer together
 - Phase 2 upgrade will impose trigger constraints on layout of RODs and mapping of FE to ROD links
 - Also no (completely) independent readout path

Design Considerations for L1Calo (1)

- We want low thresholds and rates at higher lumi
- We know we need to use finer granularity for this
 - But not sure how much better we really need
 - Or where is the best place to have it (ROD/L1Calo)
 - Or how to use it (what algorithms)
- Design ideas ought to be guided by simulation...
 - But no simulation yet
 - Instead, mainly doodles around technology limits
 - Mainly dating from before serious work on phase 1 started

Design Considerations for L1Calo (2)

- Latency:
 - Still expected to be critical
 - Assuming regional L1Track trigger requiring L0 RoIs
 - No unnecessary deserialisation/reserialisation
 - Significant latency penalty (several BCs?) at each such step
 - Some serialisation is unavoidable:
 - FE- \rightarrow ROD, ROD- \rightarrow L1, L1- \rightarrow Merger/CTP(?)
 - Avoidable: everything else!
 - Eg between RODs, between L1 modules

Design Considerations for L1Calo (3)

- Calorimeter boundaries

- Worst case (by far) is EM barrel/endcap transition
 - Anything we can possibly do will probably be needed
 - Sum cells across EMB/EMEC before making L1 primitives?
 - Add in crack scintillators? (Currently read out via Tile EB)
- Cant do anything about crack at $\eta=0$
- Next worst is Tile LB/EB transition
 - Currently cells are deliberately misorganised to adjacent η bins to avoid analogue summing across the boundary
 - Probably need to do it properly for the upgrade
 - Add in the gap/crack scintillators?
- Least worst is Tile EB/HEC transition
 - Again, currently misorganised - could do better digitally

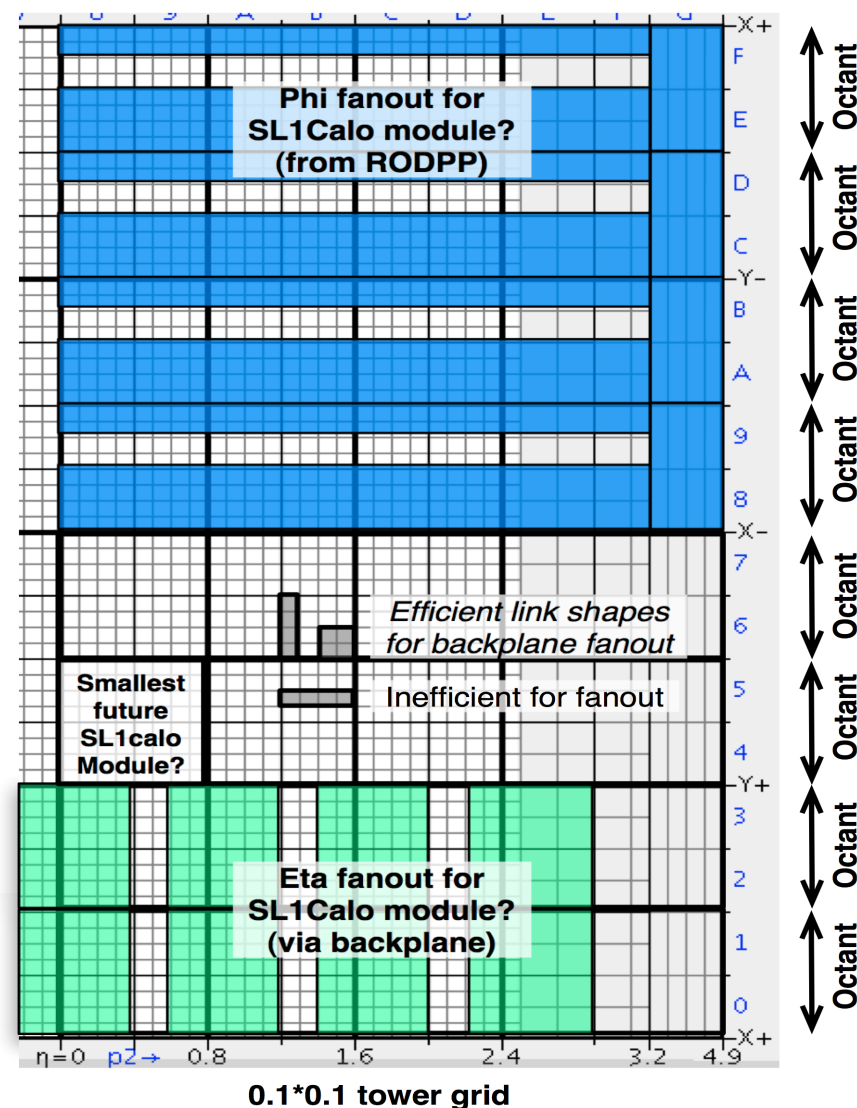
Design Considerations for L1Calo (4)

- FE and ROD mappings
 - L1 constraints will affect the layout of RODs and FE links
 - Worry about the difficult areas early in the design process
 - Do as much as possible as early as possible
- Bridging boundaries vs independent operation?
 - Tile ROD proposal spans all four of EBC,LBC,LBA,EBA
 - Good for handling boundaries in the trigger
 - But harder to calibration each partition independently?
 - Will LAr RODs span barrel/endcap boundary
 - If so, will LAr have the same problem?
 - Duplicate front end to ROD links across boundary regions?
 - Could use one copy for the trigger, the other for readout

Possible Phase 2 Architectures (1)

- Example ideas...
- Single processor module?
 - For all objects: EM, tau, jet
- Still use sliding windows
 - Unless there is a better idea?
- Fewer remapping stages?
- Consider phi octant layout?
 - Similar fanout in L1 modules
 - Unless modules wider in eta?
 - $O(75\%)$ fanout from RODs
 - Fewer restrictions on eta, phi shape covered by RODs
 - But still need regularity

Phi octant architecture and fanout



Possible Phase 2 Architectures (2)

- Extreme case 1: Minitowers, SuperL1Calo
 - Send 0.05×0.05 EM towers (middle and back layers)
 - Maybe 0.025×0.1 for PS and 0.0125×0.1 for front layers?
 - All depth samplings separate
 - Less need to organise cells in RODs
 - LAr data “reduction”: 60 cells $\rightarrow 4+8+4+2 = 18$ minitowers
 - 150 Tbits/s in to LAr RODs, ~ 30 Tbits/s out to L1Calo
 - NB bandwidth in/out ratio would vary considerably with η
 - L1Calo expands to 8 crates in ϕ octant layout?

Possible Phase 2 Architectures (3)

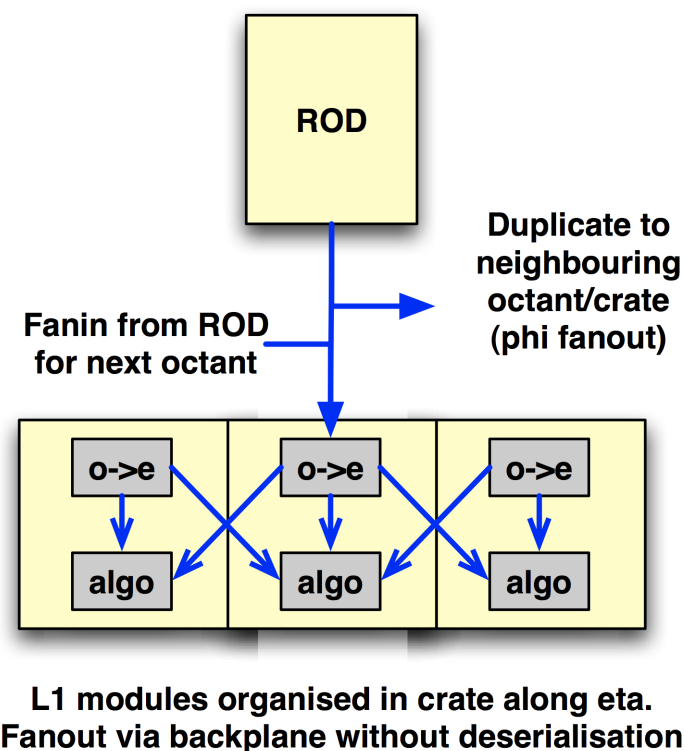
- Extreme case 2: Supertowers, miniL1Calo
 - EM shower well contained in existing 0.1×0.1 tower
 - Future LAr ROD FPGA might cover 0.2×0.2 with full depth?
 - 40 GBT links equivalent to two whole FEBs or 256 cells
 - Would need a lot of organisation of links into RODs
 - Run mini sliding window at full granularity in each ROD FPGA
 - Using L2 like algorithm?
 - Send found electrons or half electrons to L1Calo (at 0.1×0.1)
 - Another sliding window to fix up boundaries, apply hadronic veto
 - And find taus, jets, etc
 - Might squeeze low granularity L1Calo into a single crate
 - No phi fanout required for single crate L1Calo
 - Send 0.2×0.2 on one 6Gbit/s link $\Rightarrow O(2000)$ links
 - Issue: L1 algorithms moves into LAr ROD domain
 - How to collaborate on development?

Possible Phase 2 Architecture (4)

- Links from RODs duplicated to neighbouring octants
- Links to neighbouring L1 modules duplicated without reserialisation
- Example optical bandwidths
 - Including factor 2 phi fanout
 - Excluding 1.75 electrical fanout
 - Assume 0.8*0.8 trigger module

Option	Tbit/s (total)	Gbit/s (module)
EM, had towers+bits	14	200
Minitowers*samplings cf LAr ROD	60	1000 600

Fanout of data from RODs to L1



Summary

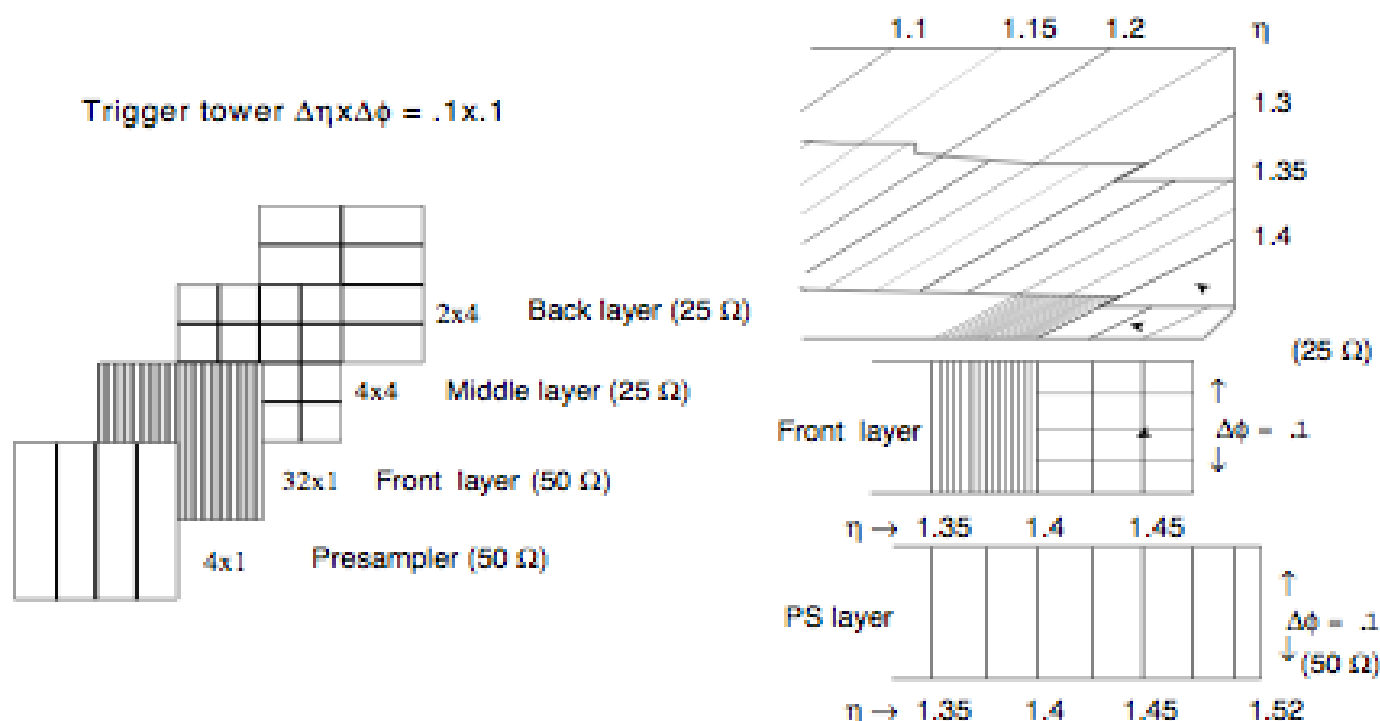
- (Much) more simulation and thought required to:
 - Identify optimal and workable algorithms
 - Derive viable L1Calo architecture in more detail
 - Decide what we will mean by a tower?
- Need to discuss implications of FE/ROD/L1 layouts
 - Limits of FPGA processing and bandwidth in ROD and L1
- Timescales?
- Who is actually going to work on all this?!

Backup Slides

EM Barrel Geometry

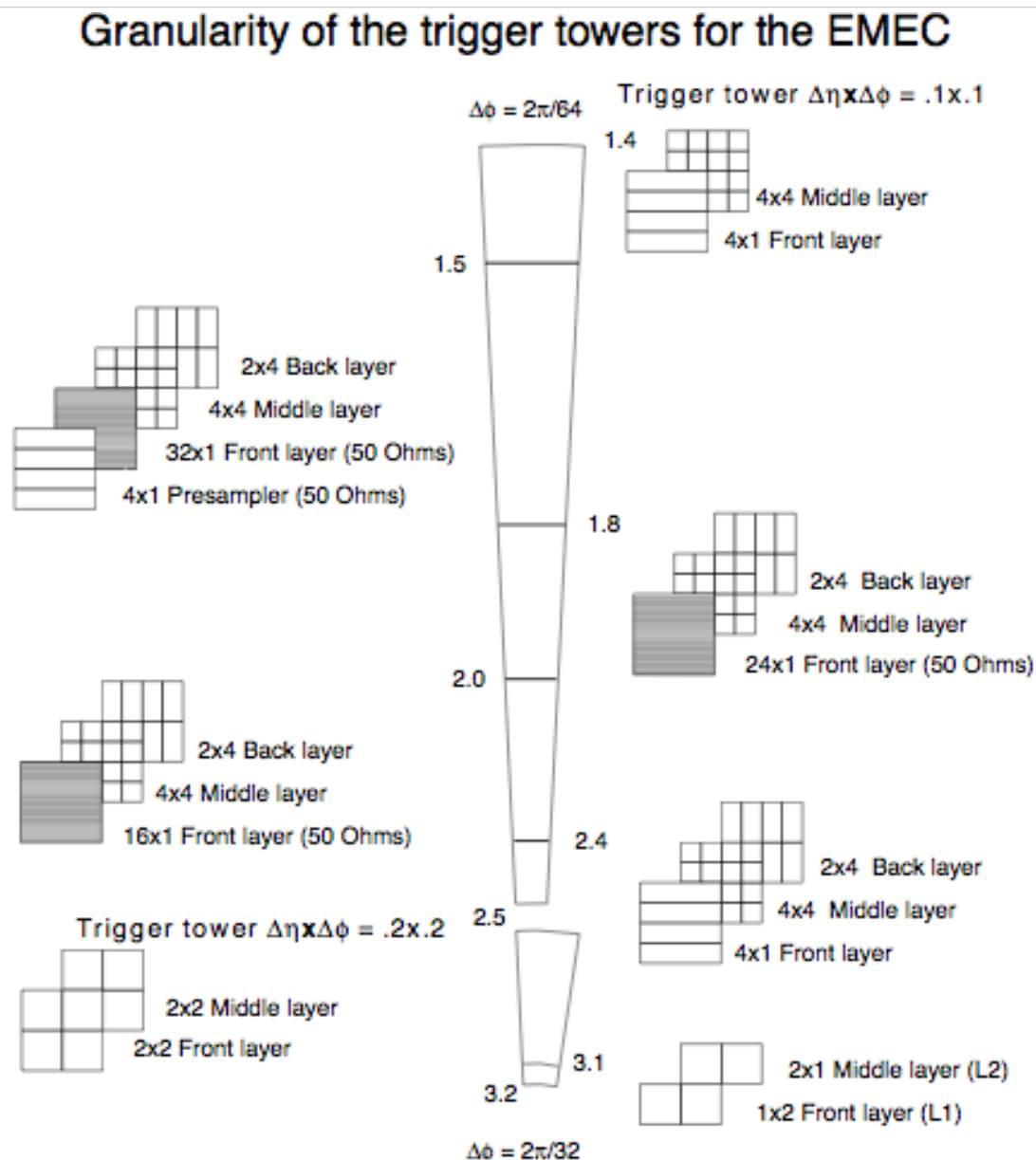
- Each layer has a different geometry
 - Uniform in eta, except for barrel/endcap transition region
- Middle and back compatible with 0.05×0.05 minitowers
- But front (strips) and presampler cover 0.1 in phi

Granularity of the trigger towers for the EMB



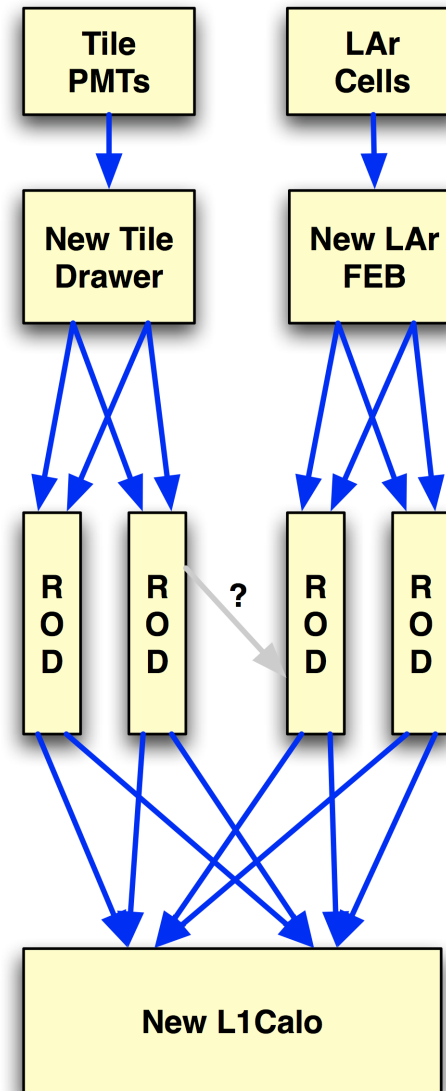
EM Endcap Geometries

- Seven different layouts between $\eta=1.4$ and $\eta=3.2$
- Many different ways cells are grouped into FEBs
 - Always(?) by layer
- NB two granularities in the EM barrel
- One in the FCAL
- (Plus similar in the hadronic layer)



Possible Upgrade Mapping Stages?

- Fewer steps available?
 - Unless we add latency with an additional reorganisation
- Start with FE boards
 - May need several different channel to link mappings?
- Remap FE to ROD links
 - Signals in depth and across boundaries to same place
- No/minimal (low latency) transfers in ROD crates?
- Regroup (and duplicate) ROD to L1Calo links



Grouping of FE cells constrained by calo geometry

Add remapping board on LAr FEB to regroup cells on links?

Regroup inputs to RODs?
Split/merge fibre ribbons?

Little data transfer between RODs?
Regroup towers on links to L1Calo

Mesh of links to L1Calo (duplicate data for phi fanout)

Any remaining mapping issues resolved by firmware

LAr Front End Board Layout

- Diagram shows eta, phi sizes of FEBs in different regions
 - Sketched on 0.1*0.1 tower grid
- Barrel, endcap & FCAL have many different geometries between (and within them)
- Transition regions span boundaries in both eta & phi
- Bring all layers to one ROD requires splitting some FEBs between two or four RODs
 - Is this a problem (in principle)?

