Timing, Trigger and Control System

Murrough Landon – 26 May 1999

- Overview
- TTC crate and optics
- TTCvi
- TTCvx
- TTCrc
- How will we use it?

TTC Overview (1)

TTC Features

- Distribute LHC clock and synchronisation signals (BC RESET) to all on- and off-detector electronics.
- Incorporate delays to compensate for particle flight times and various propogation delays.
- Deliver L1ACCEPT (and calibration triggers) to front end systems.
- Send (a)synchronous commands and data to all or individual FE systems.

TTC Overview (2)

TTC Architecture

- Tree structure: one complete tree per subdetector partition.
- Source of all signals controlled by VME module: TTCvi.
- Signals encoded and transmitted by a high power laser down a network of passive optical splitters.
- Signals decoded by ASIC at the receiver: TTCrx chip.

TTC Parameters

- Accurate timing: 55ps (cf LHC bunch length 180ps).
- Low(ish) bandwidth for commands: few μs.

TTCvi Features (1)

Clock

- Normally uses external (LHC) clock
- Otherwise generates its own 40MHz clock
- Selected clock is output from front panel

Triggers

- Normally L1ACCEPT input
- Three other NIM inputs possible
- Random trigger at 0.001, 0.1, 1, 5, 10, 25, 50 or 100kHz
- Only **one** trigger source may be selected
- Selected trigger is output from front panel

TTCvi Features (2)

Commands

- Two command channels: A and B
- A channel is reserved for transmitting L1A
- B channel can be used to send:
  - L1A event number and trigger type
  - commands/data to one/all TTCrx chips
- Bandwidth limited: synchronous commands require B channel to be free
- Otherwise commands are queued
- Minimum transmission time is 4.4μs

TTCvi Features (3)

B-Go Commands

- There are four B-Go channels
- One is reserved for BCRESET; the other three are available for users
- Series of commands may be loaded into FIFOs via VME
- These command(s) may be sent:
  - as soon as the FIFO is not empty
  - in response to VME command
  - when triggered by a front panel signal
  - synchronised to a particular LHC bunch number (optionally repeated each LHC cycle)
- A front panel signal is generated when the command(s) are sent
- Additionally, single commands may be generated from VME

TTCrx Features (1)

General

- ASIC receives encoded TTC A and B channel data
- Recovers LHC clock from the data
- Provides raw clock and two delayed versions
- Generates L1A (single bit for each BC) from the A channel with 100ns latency
- Outputs commands and data received via the B channel
- Each ASIC has a configurable ID so it can be individually addressed
- Configuration read from PROM, I2C bus, or via the TTC system itself

TTCrx Features (2)

Registers

- Configuration registers (69 bytes from PROM)
- Control register: disable unwanted features to save power
- Coarse delay register: 0-15 ticks for L1A, BCRESET and user commands
- Two fine delay registers: 0-25ns in 104ps steps for clk1, clk2
- Bunch counter
- Event counter
- Error counters

TTCrx Features (3)

Commands

- Short format (broadcast) commands: eg BCRESET and some user commands
- Long format commands:
  - typically individually addressed, but may be broadcast
  - can set internal registers (eg delays) or output data to external subaddresses

Hardware

- Packaged as 15mm ball grid array
- Rad hard version to be produced

How Do We Use It?

All our TTCrx chips will be VME addressable (I2C bus), so no need to configure them via the TTC itself?

Alternative trigger inputs for various calibrations: eg together with LAr/TileCal pulser systems?

B-Go channels useful for testing - eg load known data, start/stop pipelines and readout both ends of a link.

Also for calibrations synchronised with LHC bunches. But how does the auto repeat facility match with allocation of one in N long gaps to each subdetector?