Rack Layouts (1)

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- Considerations
- Recent Developments
- Proposed Layout
- Outstanding Issues

Considerations

- Minimise the critical latency path (Jet/Et trigger, TTC to LAr)
- Ergonomic, maintainable layout: two 9U crates per rack above separate power supplies
- Internal cables $<$ 10m

Recent Developments

- Original USA15 layout was far from ideal
- Useful negotiations with the Technical Coordination group
- Now, we have more holes through the shielding wall (two 400mm and four 300mm)
- Some services have been moved to allow a continuous central row of racks on niveau 2 of USA15

Rack Layouts (2)

Proposed Layout

- Calorimeter Trigger upstairs
- Continuous row of centrally placed racks
- Receiver crates at the outer ends connecting to PrePro-cessor and the Cluster and Jet/Et processors in the mid-dle
- Muon Trigger downstairs
- RPC and TGC triggers either side of central gap?
- CTP and TTC downstairs?

Outstanding Issues

- Confirm holes in shielding wall with TC group. We want the two 400mm holes to niveau 2 now
- Still need to confirm number, size and bending radius of cables and communicate to TC group
- Choice of cable from TileCal (to Calo and Muon triggers) still not made
- Receiver crate may require cable supports extending out-side the 1m deep racks
- Location of TGC electronics still not decided?
- What is the critical latency path? Maybe via Silicon Tracker racks in USA15?