ATLAS Level-1 Calorimeter Trigger 28 February 2001
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Calibration and Setup Procedures

Murrough Landon

1 Introduction

This document describes the calibration and setup procedures required to correctly configure the Level 1 Calorimeter Trigger [1].

The first few sections briefly describe the hardware setup and the data path through the electronics. We also summarise the calibration and configuration parameters we need to measure or check. Many of our calibration procedures require the use of the calibrations systems of the two calorimeters and we list our requirements in this area.

Following the introductory part, we then list all the calibration, setup and verification procedures we have to implement. For each one we give an outline of the procedure, its required inputs and the expected outputs. **NB not yet done in much detail**.

2 Hardware Configuration

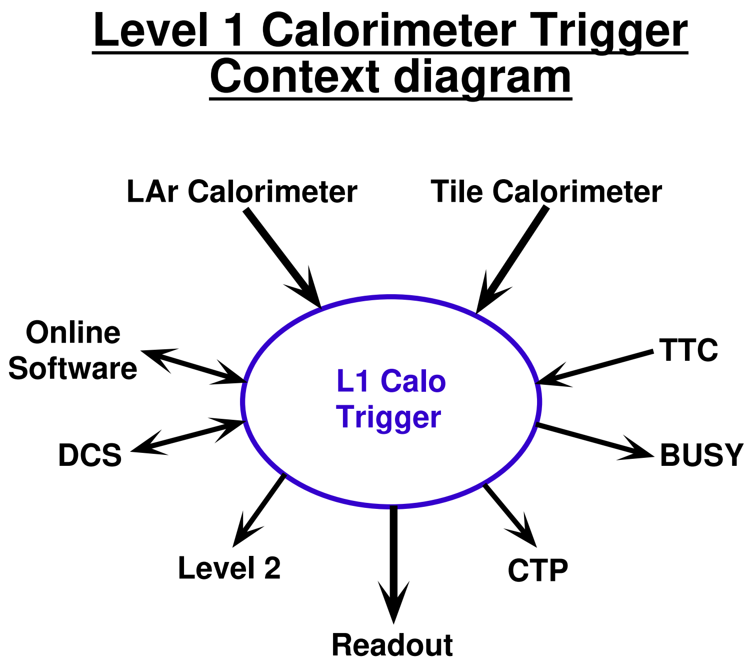
The overall context of the calorimeter trigger is shown in figure 2.

A more detailed diagram of the data path through the calorimeter electronics up to the inputs of the trigger processor is given in figure 2.

In the LAr calorimeters, the signals from the preamps are first summed within one depth layer, then these signals are summed to form the trigger towers. In the TileCal, the photomultiplier signals are amplified (**check!**) on the "3-in-1" board before being summed on a separate board to form the trigger towers.

The analogue signals from the on-detector electronics are reshaped by "receiver modules" in USA15. The LAr receivers make a small Et adjustment whereas the Tile receivers have to perform the full E to Et conversion. The outputs from the receiver modules pass via short (5m) cables to our PPM inputs.

The PPMs contain lookup tables to make the final Et calibration. They are also responsible for synchronising all the incoming data and identifying the correct bunch crossing from the calorimeter pulses which span five bunch crossings.



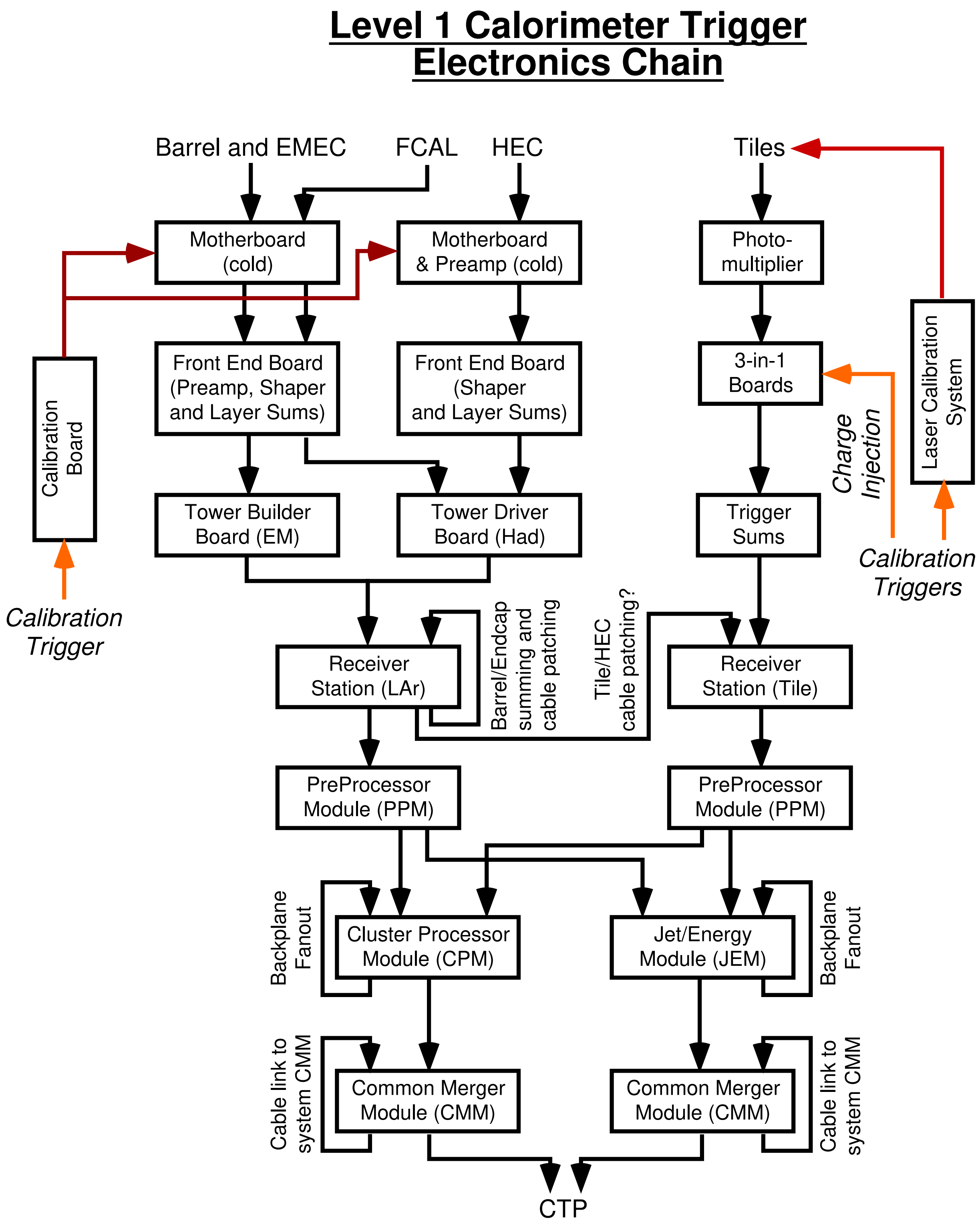
L1Calo context diagram.

3 Configuration Parameters

The complete configuration of the trigger processor requires a large number of parameters. Some of these are derived from trigger menu choices. However the bulk of them must be determined by calibration.

The complete list of parameters for each type of module is described in [3]. Below we summarise the main calibration parameters.

- Clocks: delays for the TTCrx output clock(s), possibly also some other TTCrx parameters.
- Readout: the L1Accept latency for each readout pipeline memory.
- Energy calibration: the lookup tables in the PPMs.
- BCID: the FIR filter coefficients and saturated BCID thresholds.
- Voltage levels: the FADC zero level and external BCID disriminator thresholds.
- Input timing: the FADC strobe phase and synchronisation delays.



Calorimeter trigger electronics chain.

- Internal timing: clock and strobe phases for all internal links.

4 External Requirements

4.1 Calorimeter Calibration Systems

We will need to use both LAr and Tile calibration systems. In the Tile calorimeter there is a choice of three, though only two are likely to be of any use to us, and we will most probably only use one of those.

We have the following requirements on the calorimeter calibration systems.

- Granularity: we must be able to pulse each trigger tower separately. We must also be able to effectively pulse each component cell forming a trigger tower. This may be done either by the calibration system itself or by disabling inputs to the trigger tower sums.
- Energy: we must be able to receive pulses with a range of different energies both within our dynamic range (0–255GeV) and beyond it (to study saturated pulses).
- Timing: the timing of the calibration pulses must be the same timing – within a small tolerance (about 1ns?) – of real particles.
- Synchronous: it would be desirable to be able to simultaneously pulse different areas of the calorimeter simulaneously (which may be in different TTC partitions). Eg to see signals summed across the barrel/endcap transition etc.

Initial discussions with the calorimeter groups suggest that at least the first three main requirements can be met by the LAr calibration system (havent checked the last) and also by the TileCal charge injection system. The TileCal laser calibration – I think – can only pulse all cells at once.

4.2 Online Software

The run control system [2] should allow us to operate a calibration procedure in a convenient fashion. This means the ability to start a calibration run and then iterate the following steps: take a few events, pause the system automatically, stop triggers temporarily, change some parameter throughout the system, restart triggers and resume data taking. After a specified number of iterations, the run should stop automatically.

Stepping through a sequence of parameters in a single run is probably more convenient for analysing the data in a single monitoring process than a sequence of runs which have to be analysed separately and their data combined afterwards.

To some extent though, we will have to operate in the same way that each calorimeter chooses to run. Hopefully they will not be too different from each other.

5 Summary of Procedures

The detailed procedures are listed in the appendix. This section gives a brief overview of the most important aspects.

5.1 Energy Calibration

Every channel in the PPMs contains a 1024 entry lookup table (LUT) for the energy calibration. This can be filled by downloading all 1024 values. Alternatively, if the calibration is linear, the PPrASIC can fill the LUT itself, given an offset (pedestal) and a slope.

A coarse Et correction is also performed in the LAr receiver modules to correct for some gain steps in the front end electronics. The Tile receivers will however do the full Et conversion as the Tile front ends make no Et correction at all.

5.2 Timing Calibrations

The main timing calibration is the coarse and fine timing of the input signals to the PPMs: ie FADC strobe phase and clock tick delay.

In addition to this, there are a number of internal timing setup procedures for each of the links between modules: PPM-CPM, PPM-JEM, CPM-CMM, JEM-CMM, CMM-CMM, CMM-CTP.

5.3 BCID Calibration

The pulse shape for every channel has to be measured to derive the coefficients for the matched filter. Thresholds for the satured pulse algorithm also have to be determined.

5.4 Integrity Checks

We must check that all input and internal cabling is correctly wired and functioning without faults. This includes all cabling from calorimeter cells through calorimeter electronics, receiver modules to PPMs; all internal cabling, ie the real time data paths mentioned in the timing section plus those for readout and ROI data, ie PPM-PPROD, CPM-CPROD, CMM-CPROD, JEM-CPROD, PPROD-ROS, CPROD-ROS, CPROD-ROIB.

A Calibration of Input Signals

This section covers all aspects related to our input signals. This mostly means the PPM inputs. However, although not strictly our domain, some calibrations and checks of the trigger summing and shaping chain in the calorimeter electronics can best be done via the PPMs.

A.1 Relative Calorimeter Cell Timing

In both calorimeters, several cells are summed to form a single trigger tower. In principle the cable paths from each cell to the summing boards should be equal to within our required tolerances. Nevertheless we will want to check that this is indeed the case.

Procedure: use calorimeter calibration system. Arrange to pulse one cell input per summing board at a time; other cells in the same summing board are either not pulsed or masked off. Read a sample of events for each cell from the PPMs. Iterate over the cells in each summing board. All summing boards in the system can be checked simultaneously. NB slightly different procedures may be required for LAr and Tile calorimeters?

A.2 Timing of Barrel/Endcap Summing

Towers from the LAr Barrel and Endcap in the overlap region are summed in the Receiver modules. Since the cable paths from Barrel and Endcap are different, there may be a latency different of several bunch crossings between them. This latency must be determined for each pair of signals to be summed.

Procedure: use calorimeter calibration system. Pulse Barrel and then Endcap separately, measure relative timing of signals arriving (via the Receivers) at the PPMs. Ideally we would then pulse Barrel and Endcap partitions simultaneously and checked the summed pulses. A single energy within the trigger dynamic range should be sufficient.

A.3 Timing of Tile Overlap Summing

The TileCal barrel and extended barrel both include towers covering 0.8–1.0 in eta. In the barrel these will be summed in the receiver modules to form the tower at 0.8–0.9, in the extended barrel they will form the tower at 0.9–1.0. It is hoped (**check this!**) that equal length cables in the TileCal electronics drawers will ensure that each pair of signals to be summed are in time with each other. This must be checked. Q: what do we do if its wrong? Do we anticipate delays in the receiver stations?

Procedure: use calorimeter calibration system. Pulse 0.8–0.9 and 0.9–1.0 towers separately and compare their timings at the PPMs. Ideally we would then pulse both towers simultaneously and checked the summed pulses. A single energy within the trigger dynamic range should be sufficient.

A.4 Latency of PPM Inputs

Signals from the calorimeters will arrive at the PPM inputs with varying latency. The latency (whole clock ticks) needs to be determined for every tower.

Procedure: use calorimeter calibration system. PPMs can read up to 5 bunch crossings of data (unless we can freeze their pipelines?). This is probably less than the variation in timing at least between Barrel and Endcap, EM and Hadronic sections. So we need to scan the 5 bunch crossing frame: read a few events, change the readout frame, iterate. Determine which frame contains the pulse for each tower and the latency within that frame.

A.5 Timing of FADC Strobe Phase

The calorimeter signals arriving at the PPM inputs will have varying phase with respect to the LHC clock. This phase (within one clock cycle) needs to be determined for every tower. The pulse covers about 5 clock cycles. The aim is set the FADC strobe of the central cycle at the peak of the pulse. Q: what is the required timing margin?

Procedure: use calorimeter calibration system. Assume the latency (whole clock ticks) has already been determined (A.4). Read a few events, adjust the FADC strobe by 1ns, iterate. Determine which strobe timing gives the maximum peak value and most central pulse shape. Or something like that?

A.6 Calibration of Unsaturated BCID Parameters

The unsaturated BCID algorithm uses a “matched filter”, ie the filter parameters correspond roughly to the pulse shape. The pulse shape must be measured for every tower. Reliable identication of the bunch crossing requires that the shape be independent of energy. This must be checked.

Procedure: use calorimeter calibration system. Assume the latency and FADC strobes have already been determined (A.4,A.5). Read a few events, measure pulse shape, change calibration pulse energy (within trigger dynamic range), iterate. Q: do you get a better measurement of the shape by also scanning the FADC strobe timing? Q: efficieny of BCID as a function of FADC strobe mistiming also needs to be measured.

A.7 Calibration of Saturated BCID Parameters

For saturated pulses (above about 255GeV) a different BCID algorithm is used. This applies two thresholds to the rising edge of the pulse. Safe values for these threshold need to be found for every tower. Also the threshold at which the satured algorithm should be used in preference to the unsaturated algorithm.

Procedure: use calorimeter calibration system. Assume the latency and FADC strobes have already been determined (A.4,A.5). Read a few events, measure pulse shape, change calibration pulse energy (above trigger dynamic range), iterate.

A.8 Calibration of External BCID Parameters

The analog input daughtercards on the PPMs also make provisional for an analogue “external BCID” signal based on a discriminator. The threshold for this needs to be determined for each channel.

Procedure: use calorimeter calibration system. Similar to above (A.7)?

A.9 Energy Calibration

An Et correction is applied to LAr signals in the receiver stations. The TileCal receivers also convert raw energy signals to Et. A further refinement and FADC pedestal subtraction is made in the PPM lookup tables. All these settings need to be determined for each channel.

Procedure: use calorimeter calibration system. Maybe also full calorimeter readout data from calorimeter DAQ partitions.

Presumably we first try to tune the Et calibration as well as possible with whatever analogue facilities are available in the receiver stations, then refine it using the PPM lookup tables. Iterative optimisation?

B Internal Timing Setup

This section deals with the calibration and setup of the links between various components of the trigger processor.

All towers should be aligned in time at the PPMs and thereafter the cables to other parts of the system should all be the same length. However there may be small differences which will need adjustment - and certainly need to be checked.

B.1 PPM to CPM Cable Links

The Serialisers on the CPMs can strobe the incoming LVDS data on one of four 6.25ns phases within the LHC clock cycle. There is also an optional one tick delay for further synchronisation. The best phase, and whether the extra delay is required, must be determined for each tower. The Serialisers themselves can autocalibrate the phase, however the delay must be found by comparison with other Serialisers.

Procedure: use playback data from the PPMs. Load the PPM playback memories with a repeating 0xAA,0x55 pattern to ensure adequate transitions. Synchronously start playback from all PPMs. Switch all CPM Serialisers into calibration mode, wait for all Serialisers to indicate that calibration is complete. Switch out of calibration mode and stop PPM playback. Read all chosen phases. Compare the data read from each channel of a given CPM to see if any of them require the extra delay (all should have either 0xAA or 0x55 on the same tick).

The board clock (ie TTCrx ClkDes1) may need to be adjusted to optimise the choice of phases and delays for the whole board. This may need to be done in common across the whole CPM crate to avoid problems with backplane transmission? Q: what is the tolerance for clock phase differences between boards in the same crate.

B.2 PPM to JEM Cable Links

The Input FPGAs on the JEMs use a similar synchronisation scheme as the CPM Serialisers.

Procedure: similar to that for the CPMs (B.1).

B.3 CPM to CPM Backplane Links

Each CPM sends and receives data at 160MHz from its two neighhours. The CPchips on each CPM include a calibration mode to determine the correct phase of the 40MHz clock to demultiplex the 160MHz data stream.

Procedure: use the autocalibration mode of the CPM Serialisers and CPchips. Assume the CPM board clock has been set to its optimal value (B.1). Switch all Serialisers on all CPMs in the crate into backplane calibration mode. Switch all CPchips into autocalibration mode. Wait for all CPchips to indicate that autocalibration is complete. Switch CPchips and Serialisers out of calibration mode. Read the calibrated phases from all CPchips.

B.4 JEM to JEM Backplane Links

Each JEM sends and receives data at 80MHz from its two neighhours. Unlike the CPchips, no special autocalibration mode is foreseen in Jet FPGA. Track lengths on the JEM are calculated such that the data will be received correctly - assuming, presumably that all JEM board clocks are synchronised throughout the crate?

Procedure: none required? What about checking it though?

B.5 CPM to CMM Backplane Links

Each CPM sends parallel hit multiplicities at 40MHz to the two CMMs in the same crate. Due to different backplane track lengths there will be a few ns skew between the incoming signals (plus any phase differences among CPM board clocks). The best phase to strobe all the incoming data on the CMM must be determined.

Procedure: use CPM playback memories. Assume all CPM timings have been set correctly (B.3). Load suitable patterns in the Serialiser playback memories. Synchronously start playback from all CPMs in the crate. Read a few events, change the CMM board clock phase, iterate. Determine the best clock phase.

B.6 JEM to CMM Backplane Links

The JEM to CMM communication is similar to that between CPM and CMM.

Procedure: similar to that for CPM to CMM links (B.5).

B.7 CMM to CMM Cable Links

One CMM in each of the Cluster, Jet and Energy processor chains acts as the system CMM, summing the results arriving at 40Mhz on parallel cable links from the other crates. The phase for strobing the incoming data from other CMMs needs to be determined (or at least checked).

Procedure: use CMM playback memories.

B.8 CMM to CTP Cable Links

Each system CMM sends its combined data to the CTP. The latency and phase of the data arriving at the CTP has to be measured. This is the responsibility of the CTP group, but clearly requires data from the CMMs

Procedure: use CMM playback memories.

C Integrity Checks

This section discusses the procedures for checking the integrity of the system.

C.1 Tower Formation

In all the calorimeters, trigger towers are formed by summing several calorimeter cells. In many cases, the modularity of the calorimeters and their electronics preclude gross mistakes. There may be cases (**check!**) where the possibility of cabling errors exists such that cells are summed into the wrong tower.

Checking this with the calorimeter calibration systems does however require that the the calibration system is correctly cabled... Matching errors may be difficult to detect.

C.2 Towers to PPMs: Cabling

Depending on the calorimeter, between 7 and 16 towers are grouped into each cable from the detectors to the receivers and thence to the PPMs. In principle (**check!**) this is fixed in the on detector electronics, but the trigger processors depend on this grouping being correct, so it must be checked. The bulk cabling must also be verified.

Procedure: use calorimeter calibration systems. Pulse a single tower at a time (or well separated groups of towers?), read a few events, check that the signal(s) are seen in the correct channel in the correct PPM. Iterate over all towers in the system.

Ideally, for complete confidence, the iterations should be done one tower at a time at least once at initial installation. Thereafter some more parallel checks could be repeated after any intervention in the cabling.

C.3 Towers to PPMs: Crosstalk

We need to measure the level of cross talk among, most probably, the channels within one cable connector.

Procedure: use calorimeter calibration systems. Pulse a single tower in each cable/connector at a time, read a few events, measure the cross talk seen in adjacent channels. Iterate over all towers in the system.

C.4 Towers to PPMs: Analogue Noise

We presumably need to measure the level of analogue noise.

Procedure: not sure.

C.5 Towers to PPMs: Reflections

The signal cables from the calorimeter are up to 70m long. There are also other cable links at each end. Presumably the analogue electronics is designed to minimise reflections, but this should be checked.

Procedure: use calorimeter calibration systems. Pulse all towers, read a few events. Check signal shape for reflections close in time. Shift PPM readout frame a few ticks later and iterate, looking for signals significantly later in time. Reflections in the signal cables from the front ends would arrive after about 20–30 bunch crossings. Calibration triggers should be much less frequent than this interval. NB: if PPM pipelines can be frozen this procedure could be done as a single shot capturing up to 256 timeslices at once.

C.6 PPM to CPM Cabling

Each PPM sends the bulk of its tower data to one CPM, but additionally fans out a few towers to a CPM in each neighbouring phi quadrant. Each LDVS cable groups four channels (eight BCMuxed towers) so the number of separate cables is large and the potential for miscabling is high.

Procedure: use the PPM playback memories. Load suitable test patterns in all PPMs: eg alternate ticks could contain coded crate+module (3 bits + 4 bits) and channel numbers (6 bits). Read a few events from the CPMs and check that each channel is receiving data from the correct PPM. NB this needs to be done with BCmux disabled: first transmit the first tower of each BCmux pair, then repeat the procedure for the second tower. The disabling of BCmux and selection of BCmux channels must be done at both PPM and CPM ends.

C.7 PPM to JEM Cabling

As with the CPM data, each PPM sends the bulk of its jet cell data to one JEM, but additionally fans out a few jet cells to a JEM in each neighbouring phi quadrant. Each LDVS cable transmits four jet cells each of which is summed from four input towers.

Procedure: use the PPM playback memories. Load suitable test patterns in all PPMs, read a few events from the JEMs and check that each channel is receiving data from the correct PPM. Although the playback memories contain the unsummed tower data, the same pattern for the CPMs (section C.7) can be used for the JEMs.

C.8 CP and JEP Backplanes

As part of the processor crate backplane acceptance tests, the correct wiring of the CP and JEP crate backplanes must be checked. It is envisaged that both the CPchip and the Jet FPGA will have a firmware mode which allows a large volume of data incoming over the backplane to be captured for subsequent readout.

Procedure: use the CPM/JEM playback memories and alternate versions of the CPchip and Jet FPGA algorithms. Load suitable test patterns and thresholds in all CPMs/JEMs, read a few events from the CPMs/JEMs and CMMs and check that each channel of each module is receiving data from the correct originating channel and module.

C.9 CMM to CMM Cabling

Data from each crate CMM is taken by cable to a single crate CMM acting as the system CMM. There are only a few such cables which can be checked by hand. Nevertheless an automated procedure is useful to check for damage to the cables.

Procedure: use the CMM playback memories. Load suitable test patterns and thresholds in all CMMs, read a few events from the system CMMs and check that each channel is receiving data from the correct originating module.

C.10 CMM to CTP Cabling

Four system CMMs send their combined data to the CTP which will probably live on the floor below. We must check that this cabling is correct. Also, since this is the interface between two systems, some way of checking the ordering of bits within each cable is probably desirable.

Procedure: use the CMM playback memories. Load suitable test patterns and thresholds in all CMMs, read a few events from the CTP and check that each channel is receiving data from the correct originating module, and that both CMM and CTP are using the same bit numbering.

C.11 Pipeline Bus Backplane

Readout of data from the PPMs to the PPROD is via the custom pipeline bus backplane in the PreProcessor crates. This consists partly of PCB and also some flat cable connections. We should have a procedure to verify that the pipeline bus is working correctly.

Procedure: use the PPM playback memories. Load suitable test patterns and thresholds in all PPMs, read a few events from the PPRODs and check that each channel is receiving valid data from the correct originating module.

C.12 Glink cables to CPRODs

Readout of data from the CPMs, JEMs and CMMs is via Glink cables to the CPRODs. The Glink data packets from these modules do not themselves identify the originating module. The CPROD firmware is expected to blithely encode the module addresses of incoming data on the basis of the Glink input number. It is important that the correct cabling of the Glink inputs is checked.

Procedure: use the CPM, JEM and CMM playback memories. Load suitable test patterns and thresholds in all CPMs, JEMs and CMMs, read a few events from the CPRODs and check that each Glink input is receiving data from the correct originating module.

C.13 PPROD and CPRODs to the ROS

Each ROD sends its data to the DAQ Readout System (ROS) on one Slink connection. Although each ROD packet will uniquely identify its source ROD, we should check that the physical connections are actually the expected ones. This will be required for correct subpartitioning of the system for tests.

Procedure: use the ROD playback memories. Load suitable Slink packets into the RODs, read a few events from the ROS and check that each Slink connection is as expected.

C.14 CPRODs to the ROIB

Those of the CPRODs which process ROIs will send their formatted ROI packets via Slink connections to the ROI builder (ROIB). Although the ROI packets do not uniquely distinguish between different kinds of ROI, the packets will contain the source ROD identifier, so the ordering of cables at the ROIB inputs may not be important (**check**). Anyway it can be simply checked.

Procedure: use the ROD playback memories. Load suitable Slink packets into the RODs, read a few events from the ROIB and check that each Slink connection is as expected.

D Functionality Checks

This section discusses the procedures for verifying that the whole system behaves correctly as a trigger!

D.1 Simulation: Digital Inputs

In ATLAS, before real data is available, the only sources of data for the whole trigger system will be the calorimeter calibrations systems and the PPM playback memories. The former is not really suitable for generating data which looks like real Physics.

Procedure: use the PPM playback memories. Generate a lot of test vectors containing physics events, load these into the PPMs, run the system for a while letting it generate triggers, check that the correct events are triggered and that the correct data is seen at all stages of the processor.

D.2 Simulation: Analogue Inputs

At the slice tests, we have the possibility of feeding our own analogue pulses into the PPMs. Some simulation of physics like clusters might be possible. Schemes which permit a large volume of data have been discussed (ie many more than the 256 time slices of the PPM playback memories).

Procedure: similar to the above (D.1).

D.3 Simulation: Subsystems

Parts of the complete system can also be tested and simulated in isolation.

E Other Stuff

What is unclear, what have I forgotten...

- Energy calibration: receivers vs PPM LUTs
- FADC pedestal
- Analogue noise
- etc?

References

[1] ATLAS Level 1 Calorimeter Trigger: home page
`http://hepwww.pp.rl.ac.uk/Atlas-L1`

[2] ATLAS Online Software Run Control component
`http://atddoc.cern.ch/Atlas/DaqSoft/components/runcontrol`

[3] Configuration Data for the ATLAS Level 1 Calorimeter Trigger (ATL-DA-EP-02)
`http://edmsoraweb.cern.ch:8001/cedar/doc.page?document_id=111349`