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Level-1 Calorimeter Trigger: Cable Mappings and Crate Layouts from Analogue Inputs to Processors

L1Calo Group [1]

1 Introduction

The purpose of this note is to summarize the cable naming conventions and specify the connectivity of the Level-1 Calorimeter Trigger system for the real time signals from the analogue cables entering USA15 right through to the LVDS signals which form the input to the main algorithm processors in the system. These cables form the bulk of the cables needed in the system.

The cables entering USA15 all carry analogue signals, and the basic route for these is through receivers, which condition and re-map the signals to be output onto further analogue cables which are fed into the Level-1 Preprocessor Modules (PPMs). The PPMs output digitized signals to the processor systems — more precisely to the Cluster Processor Modules (CPMs) and the Jet/Energy Processor Modules (JEMs). The reason for including these digital cables in this note is that to fully understand the rationale of the signal order presented to the PPMs, it is necessary to see how they are routed to the processors.

The main sources of information used to compile this information are several documents written by Bill Cleland. One of these covers the cabling of the Liquid Argon Receiver system itself [1], and the other two detail the signal pin usage of the input cables, one covering the electromagnetic part of the Liquid Argon detector [2], and the other covering the hadronic endcaps and forward calorimeters [3]. For the Tile Calorimeter inputs, the equivalent information is obtained from the TileCal Patch Panel Specification [4]. The remaining major source of information is Appendix A of the PPM specification [5].

[1] Please send any comments and corrections to Stephen Hillier.

2 Overview of Connectivity

A very good overview of the complete Level-1 Calorimeter trigger contents and connectivity is available as a web page [6]. This section extracts the information from that source which is relevant to this document.

The basic signal routing of interest is:

- detector cables to receiver inputs
- receiver re-mapping on receiver remapping boards
- receiver outputs to PPMs
- PPM outputs to CPMs and JEMs

However this relatively simple picture is complicated by several factors, mostly related to the re-mapping of signals from the detector outputs to the PPM inputs. In principle, most of this re-mapping can be achieved in the receiver remapping boards. However, there are some areas where other measures are needed. This necessitates the use of several types of patch panel to achieve the additional re-mapping. These occur in three places in the system:

- tile calorimeter input cables
- summing patch panels between receivers
- receiver to PPM cabling

This organisation is illustrated in figure 2. All Liquid Argon input cables go directly into receivers, whereas all Tile Calorimeter signals must go via patch panels (Tile Calorimeter Patch Panels, or TCPP [4]), where the muon trigger signals are siphoned off. The majority of the receivers send their outputs onwards towards the PPMs, but in a few cases, some signals are routed back into different receivers via the Summing Patch Panels. Also some receiver outputs have to go through different patch panels (Receiver to Preprocessor Patch Panels, or RPPPs) before being received by the PPMs. All PPM outputs go directly to the processor modules without re-mapping. It is this requirement that means that so much work has to be done before the PPM to produce the signal ordering required by the processors.

A general idea of the quantity of cables and modules/patch panels are given in this section, before the actual naming and connectivity is introduced in later sections.

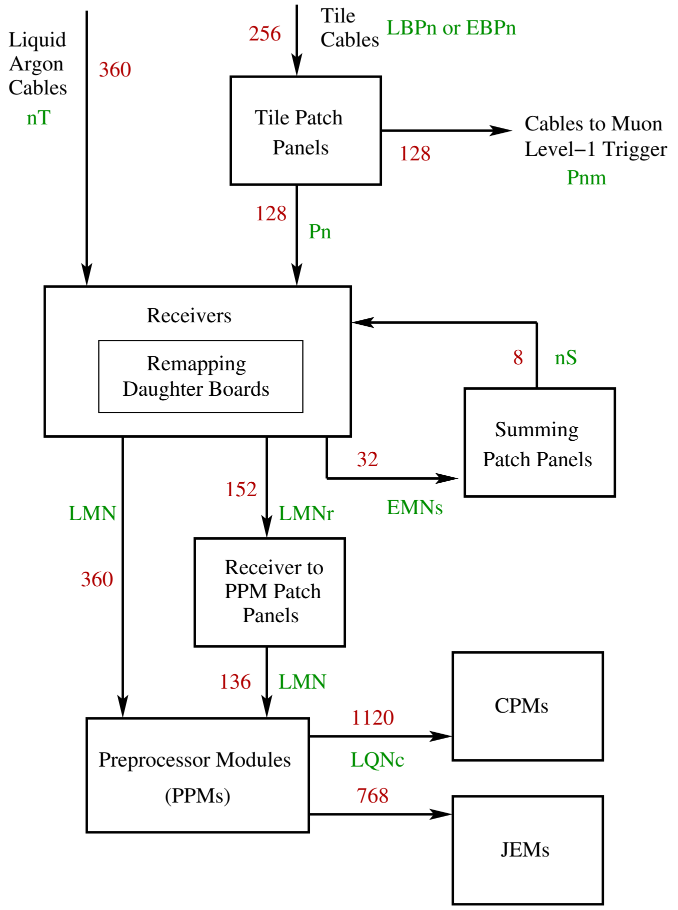


Figure 2: An overview of the cables and patch panels showing numbers of each type of cable required, and generic lables for cable types – labels are explained in section 3

2.1 Detector input cables and Tile patch panels (TCPP)

From the Liquid Argon calorimeter, cables containing 16 pairs of differential analogue signal pairs are used throughout, although not all parts of the calorimeter need all 16 pairs. All of these signals are routed directly to the receivers. In the case of the Tile Calorimeter, signals are presented in the trigger cavern on 50 pin connectors, and again all signals are carried on differential pairs. These cables are sourced at either the barrel (long barrel, LB) or extended barrel (EB) region, and include the muon signals. This means that patch panels are needed to separate off the calorimeter and muon trigger signals, and repackage the outputs onto cables with the standard 37 pin connectors used for the Liquid Argon signals. Each logical segment of the patch panel will take two cables (one from the barrel and one from the extended barrel for a particular phi/eta region), and output two cables, one to go to the calorimeter receivers, and one to go to the muon trigger system. There are 128 of these logical units required (64 phi regions for each end of the detector, A or C). Two identical units are built into one physical PCB, taking 4 input cables and providing four outputs — see the TCPP specification [4].

The quantities of cables required, and their usage of the 16 possible pairs is given in table 1. It can be seen that 616 long cables from detector to USA15 are required, and a further 256 short cables for the outputs of the Tile patch panels. Half of these will be very short — going to the calorimeter trigger receivers, and the other half will be longer, needing to go down to the lower level of the electronics barracks to the muon trigger system.

Long Cables	Num pairs	Number of Cables		
Source	required	C Side	A Side	Total
LAr EM Barrel	15	64	64	128
LAr EM Endcap	16	56	56	112
LAr HEC	16	48	48	96
LAr FCAL	16	12	12	24
Tile Barrel	9 (7)	64	64	128
Tile Ext. Barrel	6 (4 + 2 crack)	64	64	128
Total		308	308	616
Short Cables				
Tile EM Trigger	15	64	64	128
Tile Muon Trigger	(11 + 2 crack)	64	64	128

Table 1: Detector input cables: number and pair usage — bracketed figures are for muon trigger and other non-calo trigger signals

2.2 Analogue Receiver System

The receiver system is described in detail elsewhere [7, 8]. Essentially it consists of eight receiver crates (6 for LAr and 2 for Tiles), each of which contains 16 receiver modules. Each module can receive 64 of the differential analogue signals, which are connected through 4 detector input cables. The modules condition the signals, and the signals can be re-mapped through the remapping daughterboard, of which there can be several designs to achieve different re-mapping goals. The output is again via 4 cables, of similar type to the input cables (16 pairs of analogue signals). Not all of the inputs and outputs are used in all modules.

On some versions of the remapping daughterboards, summing of signals is performed. This is needed in two places: a) in the overlap region between the Liquid Argon barrel and endcap, and b) in the Forward Calorimeter, where too many signals are produced for the PPMs to process, so they are reduced in number by summing in the receivers. In the first case, summing has to be done between signals received (initially) on two different receivers. This is achieved by outputting a small number of signals on a fifth output cable (which is only used in this one exceptional case) of 4 channels. These signals are then combined via the summing patch panels onto standard 16 pair cables, and sent back into a different receiver. There are 8 summing patch panels (4 quadrants * 2 ends) each of which processes 16 channels, needing 4 input cables, and producing one output cable. There are therefore 32 of the small 4 pair cables, and 8 of the the standard cables. The length of these cables needs to be determined precisely so that the sum will be between signals from the same bunch crossing.

2.3 Receiver to Preprocessor cabling

Like the receivers, the PPMs process 64 input signals coming from 4 input cables and, in general, one Receiver output cable carries 16 signals to one PPM input. However there are four regions where special arrangements are required either combining or splitting cables. These are at the inputs of PPM_4, PPM_7 and hadronic PPM_9s, where the PPM numbering is taken from the PPM specification [5]. The repackaging of signals will be achieved via patch panels. Note that there are similar, but generally not identical, patch panels dealing with the situations at each end of the detector.

In a little more detail, the four regions are:

- PPM_4 (EM): the EM barrel/endcap transition requires that two receiver outputs (of 8 signals) are combined to a single PPM input. There are 8 EM instances of PPM_4 (2 ends * 4 quadrants) making 32 special PPM input cables from 64 receiver outputs, dealt with by 32 identical patch panels.
- PPM_4 (had): the TileCal/HEC transition is more complicated. Here one HEC output cable must be split into four sets of 4 signals and combined with four TileCal receiver outputs (each providing 12 signals) making four PPM inputs. There are 8 hadronic PPM_4s (2 ends * 4 quadrants), making 32 PPM inputs coming from 40 receiver outputs, via 8 similar patch panels.
- PPM_7 (both): here one receiver output of 16 signals is split into two PPM inputs of 8 signals in both EM and hadronic layers, ie 64 special PPM input cables from 32 receiver outputs, using 32 similar patch panels.

- PPM_9 (had): each hadronic FCAL PPM input comes from combining two receiver outputs providing 8 signals each. There are two hadronic PPM_9s in the system, so this represents 8 PPM input cables from 16 receiver outputs, needing 8 identical patch panels.

The total number of cables needed is summarized in table 2. The standard cables from the receivers to PPMs are likely to have similar lengths in general, but those to patch panels may have quite different lengths and routings, depending on the rack layout.

Cable Type	Patch Panels	Receiver to PPM	Receiver to Patch Panel	Patch Panel to PPM
Standard cables	—	360	—	—
PPM_4 (EM)	32	—	64	32
PPM_4 (had)	8	—	40	32
PPM_7 (EM + had)	32	—	32	64
PPM_9 (had)	8	—	16	8
Total	80	360	152	136

Table 2: Receiver to PPM cabling: Numbers of patch panels, direct and indirect connections

2.4 The Preprocessor system

There are 8 preprocessor crates which contain 14 or 16 Preprocessor modules, there being 124 PPMs in total. The modularity is explained later in section 7 and Appendix E. The input cabling is organized such that the signals increase monotonically in eta through several groups of PPMs within each crate. The region of eta-phi space covered by the eight PPM crates maps closely (but not exactly) to the regions covered by the eight receiver crates. The only differences come in the distribution of the modules containing FCAL signals. Each PPM processes 64 channels from 4 input cables, and these are organized in a specific and, as far as possible, consistent pattern in eta/phi space. This is the requirement that drives all the re-mapping specifications. Each PPM is identical, and there is no programmable re-mapping of channels possible in the module, so the signal order of the inputs uniquely defines the output signal order.

2.5 Preprocessor cabling to CPMs and JEMs

The outputs of the PPM are LVDS signals which are packaged onto cable assemblies which contain 4 differential pairs of signals. Some fanout of channels is required as input to the processor systems, and some data reduction is also performed in the PPM, so that the number of signals sent to the processor systems is not 64 per PPM. There are actually 10 cables which go to the cluster processing system, but not all of these go to the same CPM. The eight central signals form the core input of one CPM, and the two extra outputs are needed for CPMs processing the adjacent quadrant in phi. Only the central region of the detector ($|\text{eta}| < 2.5$) is processed by the CPMs, so only 112 (7*16) PPMs have LVDS cables connected to their 10 CPM outputs. Thus the total of PPM to CPM cables is 1120. This corresponds to 56 CPMs each taking 20 input cables.

The situation for the JEM outputs is a little more complex, with the barrel region requiring 6 LVDS output cables, but special cabling in the far eta region means that 6 further outputs are required. Details can be found in the PPM specifications [5] and Appendix E. Not all of these outputs are connected for all PPMs. In particular, for the same 112 PPMs that have CPM output, the standard 6 outputs are connected. That makes 672 standard cables (112*6). For eight of the other PPMs, dealing with the endcaps, the six standard outputs, plus two of the special outputs are connected. This makes 64 cables (8*8). For the final four PPMs, which deal with FCAL signals, again eight outputs are needed, but these are now the four central 'standard' signals, plus four of the special ones. This makes 32 cables (4*8). The total number of PPM to JEM cables is therefore 672+32+64 = 768, which corresponds to 32 JEMs each taking 24 input cables.

3 Naming Conventions

We have now dealt with the basic quantity and purpose of the cables and patch panels. Now we have to address the details of naming cables and specifying connectivity. There are different naming conventions for different parts of the system, and part of the point of this document is to be able to translate from one to another. This section sets out all the conventions relevant to this document. The final part summarises all the generic labels used, and their bounds, and can be used to interpret the names given in figure 2. One common theme is that the 'n' always labels a range of numbers.

3.1 Analogue Cable Connectors

In order to understand the connectivity of the analogue data at the individual signal level, rather than just cable level, one has to define the connector pin usage for the analogue cables. Standardised cables will be used whereever possible, and the pinout will also be standardised — this is true for the Liquid Argon Cables, the outputs of the TCPPs and everything beyond the receivers. Those standard cables are described below. The inputs to the TCPPs (Tile Calorimeter Patch Panels) are on a different type of 50 pin connector. Pin usage for these cables is detailed in table 3.

There are 16 signals carried on twisted pairs in the standard analogue cables. The connectors at both ends are SUB D 37c connectors (male), which have 37 available pins. The 5 spare pins are used for grounds. For the purposes of this document, the 16 signal pairs are labelled 1–16. This is consistent with the most frequent uses of this label in all the reference documentation. However, in some documents the convention 0–15 is used, so care is needed when comparing with information using this convention. The assignment of pair wires to connector pins is shown in figure 3.1.

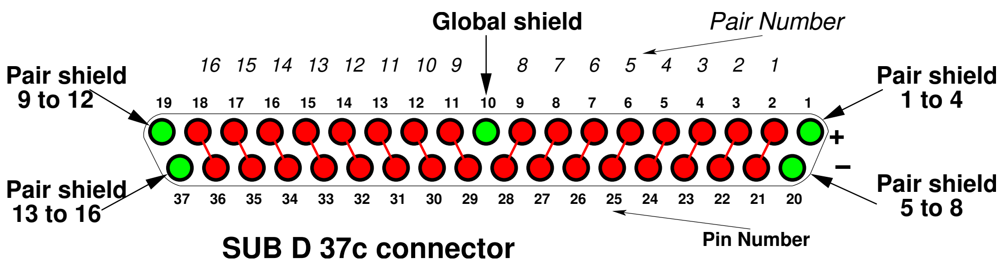


Figure 3.1: Connector pin usage on standard analogue cable

Reference Number	Pin Pair Number	Barrel Usage	Extended Barrel Usage
1	1/34	EM 0.8–1.0	EM 1.4–1.6
2	2/35	EM 0.7–0.8	EM 1.3–1.4
3	3/36	EM 0.6–0.7	EM 1.2–1.3
4	4/37	EM 0.5–0.6	EM 1.1–1.2
5	5/38	EM 0.4–0.5	EM 1.0–1.1
6	6/39	EM 0.3–0.4	EM 0.8–1.0
7	7/40	EM 0.2–0.3	Crack #1
8	8/41	EM 0.1–0.2	—
9	9/42	EM 0.0–0.1	—
10	10/43	Muon 7	Muon 4
11	11/44	Muon 6	Muon 3
12	12/45	Muon 5	Muon 2
13	13/46	Muon 4	Muon 1
14	14/47	Muon 3	Crack #2
15	15/48	Muon 2	—
16	16/49	Muon 1	—

Table 3: Pin usage for the 50 pin Tile Calorimeter input cables

3.2 Liquid Argon Input

The naming here is based on the number of the Tower Builder Board (TBB) or Tower Driver Board (TDB) in the liquid argon trigger signal builder systems. The TBBs cover the electromagnetic part of the system, and the TDBs deal with the hadronic endcap and FCAL. There are 120 TBBs, each with two output cables, which are labelled A or B. Thus there are 240 cables which are labelled nT, where n=1–120, and T=A/B. There are 20 TDBs, and these have six output cables, labelled A–F. In order to avoid confusion with TBB outputs, these are numbered 121–140. Thus there are 120 more cables labelled nT, where n=121–140, T=A/B/C/D/E/F. In all this make 360 cables, which corresponds to the figures in table 1.

3.3 Tile Calorimeter Input

There are 256 trigger cables from the Tile Calorimeter, 64 for each phi sector in the 4 eta blocks of the detector. They are numbered in the style LBPn or EBPn, where P=A/C (for endcaP), and n = 1–64. LB stands for Long Barrel, EB stands for Extended Barrel, P = A or C corresponds to A or C side of the detector, and the number n corresponds to the phi position around the detector, numbering from phi=0 and going up in steps of $\sim$0.1 (also the tile drawer number). This naming applies to the direct inputs to the Tile patch panels (TCPP). The outputs are called Pn(m) where Pn has the same meaning, and the suffix is optional. When it is left out it means the electromagnetic trigger output, and the suffix is m for muon output.

3.4 Summing patch panel to receiver cables

There are eight receiver inputs that come from the summing patch panels rather than directly from the detectors. These are the outputs of the summing patch panels which carry electromagnetic barrel signals that must be summed with endcap signals in the receivers. The simple convention used to label these is nS, where S stands for Summing, and n can run from 1 to 8.

3.5 Receiver to PPM cables

The system here was essentially invented by Bill Cleland for the receiver outputs and proposed in his receiver system note [1], but had some adaptations and additions imposed in order to clear up some ambiguities in the PPM inputs. The system is well described in that document, but a rationale and summary is given here.

The basic idea comes from the fact that most of the receiver outputs had to be grouped in 4 by 4 bundles of trigger towers in eta/phi space. This meant that the main $|\text{eta}| < 3.2$ region can be covered by a two-coordinate hexadecimal numbering system, starting from 0 at negative eta and zero phi. With the addition of a letter to indicate which layer (electromagnetic or hadronic), all cables could be uniquely labelled except for the FCAL. This system was adapted to include FCAL by adding new non-hexadecimal labels Z and G (G being one further than F, Z one 'less than' A), and also by the addition of a suffix to help to identify 'irregular' cables, where the simple 4 by 4 grouping breaks down, and patch panels need to be used.

So the final system can be summarized thus: label LMN(r), where L=E/H to indicate layer, M=0–F to indicate phi, N=Z,0–F,G to indicate eta. The optional r suffix is only used when cables are special in some way. The possible values and meanings are:

- b or e — barrel and endcap parts of transition region to be merged (PPM_4 region)

- s — sum outputs to go to summing patch panel (PPM_4 region, electromagnetic)
- o — cable containing an octant of data that needs to be split (PPM_7 region)
- x or y — the two hadronic FCAL layers to be merged (PPM_9 region)

The final inputs as they are seen by the PPMs are shown in figure 3.5 for the electromagnetic half of the system. The hadronic is very similar only with all the initial E labels replaced by H's. Note that the correspondence of this numbering system both with eta/phi location and PPM numbering is shown.

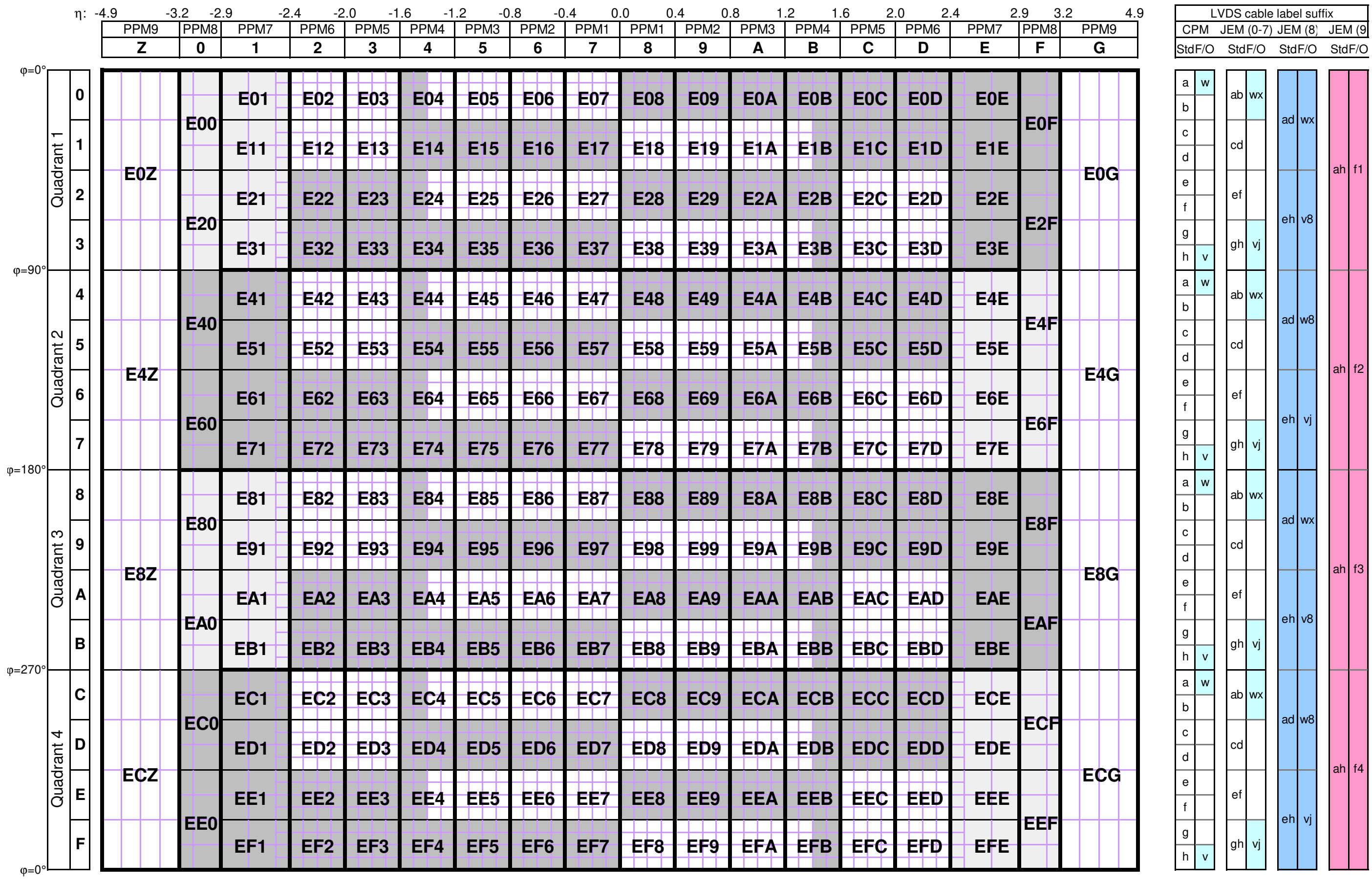


Figure 3.5: Illustration of Receiver–PPM cable numbering scheme for the EM layer. Thick solid lines show PPM modules and thin solid line PPM input cables. Light dotted lines are PPM input channels (trigger towers)

3.6 PPM to processor system cables

Here the convention builds on the ideas used for the PPM inputs, and adds in the labels used in the PPM specifications [5] for outputs to label the LVDS cables. The output labels are of the form LQNc where:

- L = E/H — for EM or hadronic calorimeter signals (layer)
- Q = 1–4 — for the quadrant number
- N = Z,0–F,G — for the eta index, as before Z means negative eta FCAL, and G is for positive eta FCAL
- c = connector — see below

The quadrant numbering scheme is that the first quadrant (1) in phi is from $0°$ to $90°$, and numbers go up to 4 in the positive phi direction.

There are 25 possible connector names and only 22 PPM LVDS outputs! This is because in the extreme eta regions, the convention dictates that some outputs are connected to a cable with a different name. The situation is shown in the far right hand side of figure 3.5, and also the names and connections are summarized in table 4 for the various regions of the system. The output connectors from the PPMs are labelled with the normal connector name plugged into that connector. Physically the connectors run downwards on the module backplane in the same order as in the table. The basic numbering scheme conforms to that used in the CPM specifications [9], and the JEM specifications [10], and is described below.

The labelling is based around a phi naming scheme within a single detector quadrant which runs from A-H, in steps of $\sim$0.2 in phi in the positive direction. The CPM input cables carry signals blocks of 0.2 in phi and 0.4 in eta (which corresponds to the 'eta width' of a single PPM). Thus each can be uniquely labelled with one of the letters A-H, there being eight such 0.2 by 0.4 blocks in each PPM. This covers the core region of eight LVDS cables. The other two PPM outputs for the CPM processor system are fanout needed to provide the trigger tower environment for the CPMs processing adjacent quadrants. These are called V and W, V being a strict copy of the H output, and W a copy of the A output. The reason for the choice of V and W is that only one phi row of the V signal is actually used by the CPM, but both are used in the W cables. This naming covers all the CPM LVDS cables. Note that for the cables themselves, lower case letters are used, whereas internally to the modules, capitals tend to be used.

For the JEM cables, the situation in the central region (PPMs 1 to 7) is similar to the CPM scheme, except for the fact that each LVDS cable covers a 0.4 by 0.4 region in eta/phi space — again the complete 'eta width' of the PPM, but now

PPM output connector	Standard PPM (1 to 7)	PPM 8 outputs	PPM 9 outputs
W	w	—	—
A	a	—	—
B	b	—	—
C	c	—	—
D	d	—	—
E	e	—	—
F	f	—	—
G	g	—	—
H	h	—	—
V	v	—	—
F1	—	—	f1
F2	—	—	f2
V8	—	v8	—
WX	wx	wx	—
AB	ab	ad	ah
CD	cd	eh	ah
EF	ef	ad	ah
GH	gh	eh	ah
VJ	vj	vj	—
W8	—	w8	—
F3	—	—	f3
F4	—	—	f4

Table 4: PPM to processor cabling: connector allocation depending on eta region

double the size in phi. Thus a single cable can carry, for example, the A and B signals for one PPM. So the core region now consists of four cables called AB, CD, EF and GH. The top and bottom fanout is done in two cables — WX, which is a copy of AB, and VJ, which is a copy of GH. In a similar way to the CPM processor, only half of the VJ signals are actually needed for the Jet algorithms.

The far eta region needs extra labels both for the special PPM–JEM outputs and to distinguish standard outputs which carry signals of a different nature. In the case of PPM_8, as can be seen from figure 3.5, each PPM covers two quadrants rather than one. This means that each JEM output cable covers an octant in phi. To indicate this altered usage of the standard output cables, the labels 'ad' and 'eh' are used for the cables. Note that there are two of each of these connected to each PPM_8, but these cables are now distinguished by their quadrant number in the scheme described above. The fanout WX and VJ cables are also connected here, with no change of name, and two special outputs are also needed. These are called V8 and W8, with the names deriving from the fact that they achieve the same fanout needs as the vj and wx cables, but cover an octant, hence the 8 in the name. These outputs are not simple copies of any of the other outputs, and the details of their signal assignment can be found in the PPM specifications [5].

Finally the PPM_9 region covering the FCAL is different again. Now each PPM covers the full phi region (ie there is only one PPM of this type per endcap A or C and per layer EM or hadronic). To indicate this, the core output LVDS cables are now all labelled ah, and four new special fanout outputs are needed. These are called F1, F2, F3 and F4, where the number indicates the quadrant number of the JEP system where the fanout is needed. Like the special far eta region fanout, the signals included here are not a direct copy of any of the 'standard' outputs.

3.7 Summary of Generic Labels

There are several generic cable labels shown in figure 2. These are listed below:

- nT
- LBPn, EBPn, Pn, Pnm
- nS
- LMN
- LMNr
- EMNs
- LQNc

Most of the individual components that make up these labels is described below, along with their possible values or fixed meanings in some cases:

- n — A number, range depending on usage (eg 1–140 for LAr inputs, 1–64 for Tile inputs, 1–8 for sum cables)
- T — TBB or TDB output connector, A or B for TBBs, A/B/C/D/E/F for TDBs
- LB — Tile long barrel input
- EB — Tile extended barrel input

- P — Endcap, A or C
- m — muon trigger signal
- S — summing patch panel output
- L — calorimeter layer, E or H
- M — phi region, hexadecimal value, 0–9,A–F
- N — eta region, extended hexadecimal value, 0–9,Z,A–G
- r — irregular receiver output to patch panel, b/e/x/y/o/s
- E — electromagnetic signal
- s — special sum output from receiver
- Q — quadrant number, 1–4
- c — connector identifier, 25 possible values

4 Receiver Crate Organisation

The configuration of all the Liquid Argon receiver crates is documented in [1]. However, this only covers 6 of the 8 crates that make up the Level-1 receiver system, so for completeness, this information is repeated in Appendix A, and also the two Tile crates are documented.

The numbering of the crates is based on a simple system mostly derived from Bill Clelland's conventions. The numbering is also used as a guide to PPM crate numbers. The receiver crates are numbered 1–8, and the correspondence between these crates and the regions of the detector are shown in table 5. The only oddity of module placement is that the first layer of the FCAL (electromagnetic layer) is actually in the hadronic crates. Each crate contains 16 modules, grouped into 4 sets of 4 modules each dealing with a single quadrant, except in the case of the hadronic endcap crates, where only 3 modules handle each quadrant and the spare four slots are used for some strange regions (FCAL and barrel/endcap transition).

Crate Number	Layer	Region	Side	Source
1	electromagnetic	barrel	+Z	LAr
2	electromagnetic	barrel	-Z	LAr
3	electromagnetic	endcap	+Z	LAr
4	electromagnetic	endcap	-Z	LAr
5	hadronic	endcap	+Z	LAr
6	hadronic	endcap	-Z	LAr
7	hadronic	barrel	+Z	Tile
8	hadronic	barrel	-Z	Tile

Table 5: Crate numbering for Receiver and PPM crates

5 Receiver Remapping Daughterboards

Although the full module and cable assignment details are covered in Appendix A, there is one more configuration detail that is needed to specify the receiver system, and that is the connectivity of the remapping daughterboards. The input signals from the detectors come in a pre-determined pinout on the cables, and the PPM system requires a consistent cable pin assignment on its input cables, as documented in the PPM specifications [5]. Essentially the signals coming in to each PPM must have, as far as is possible, the same arrangement in eta/phi space with translational symmetry across the whole detector. The basic pattern of pinouts for one standard PPM input cable is shown in table 6. This pattern has to be distorted a little at extreme eta, but is maintained across all of the central region.

Increasing Phi Steps	Increasing Eta Steps 0	+1	+2	+3
0	16	15	12	11
+1	13	14	9	10
+2	4	3	8	7
+3	1	2	5	6

Table 6: PPM input cable standard pin assignment in the central region, both eta and phi increase in steps of 0.1

The consequence is that in general there is only one possible correct mapping of signals from receiver inputs to outputs for any specific detector geometry. This mapping varies between different ends of the detector (since the input signals tend to have reflectional symmetry in eta between ends rather than translational symmetry), and also in different regions (barrel, endcap and transition areas) where detector geometry can be quite different. The far eta region, where signals start to cover larger areas in eta/phi than the standard 0.1 by 0.1 towers, also requires different treatment. In all, 22 different regions can be identified, requiring up to 22 different remapping daughterboards. These daughterboards are identified by a number running from 1–22, where the sequence follows a similar logic to the crate numbering. Table 7 identifies the regions corresponding to each number, and this table should correspond closely to those given in Table 2 of the Liquid Argon receiver specifications [7]. The tables in Appendix A show the daughtercard number needed in each receiver module.

The necessary numbers of each of these daughterboards is also listed in table 7. It would be possible to reduce the number of unique daughterboard specifications required at the cost of making the patch panels more complex, but since most of the daughterboards are fairly simple objects, it was thought best to keep the patch panels as simple as possible, and retain the 22 different types of remapping geometries. However, some economy of numbers of types was possible in the barrel region due to the similarity of the LAr and Tile geometry there. Details are given in section 5.1. A description of each of the daughterboards and their exact remapping specification can be found in Appendix B.

For those boards where signals go directly to PPMs, the necessary re-mapping is unique. However, for cables that go to patch panels, some flexibility is possible. The pinout of these cables was chosen to try to make the patch panel mapping as

Daughtercard Number	Layer	Region	Side	Number Needed
1	electromagnetic	barrel	-Z	16
2	electromagnetic	barrel	+Z	16
3	electromagnetic	transition	-Z	4
4	electromagnetic	transition	+Z	4
5	electromagnetic	endcap	-Z	8
6	electromagnetic	endcap	+Z	8
7	electromagnetic	extreme eta	-Z	4
8	electromagnetic	extreme eta	+Z	4
9	electromagnetic	FCAL 1	-Z	1
10	electromagnetic	FCAL 1	+Z	1
11	hadronic	barrel	-Z	16
12	hadronic	barrel	+Z	16
13	hadronic	transition	-Z	1
14	hadronic	transition	+Z	1
15	hadronic	endcap	-Z	8
16	hadronic	endcap	+Z	8
17	hadronic	extreme eta	-Z	4
18	hadronic	extreme eta	+Z	4
19	hadronic	FCAL 2	-Z	1
20	hadronic	FCAL 2	+Z	1
21	hadronic	FCAL 3	-Z	1
22	hadronic	FCAL 3	+Z	1
Total				128

Table 7: Receiver daughterboard numbering scheme.

simple as possible. So, for example, where two receiver output cables have to be merged into one PPM input cable, the pinout of the PPM cable is fixed, but that of the receiver cables is not. In this case, for each signal the pair assignment on the receiver output has been chosen to match the destination pair on the PPM cable.

5.1 Receiver Rear Transition Modules

As already mentioned in the last section, some re-use of daughterboards was possible in the case of barrel remappings. This is not because the receiver input to output mapping is identical, but because the differences are minor and handled in the Rear Transition Modules which receive the input signals, rather than in the remapping boards themselves. There are only two types of rear transitions modules, which are quite simple in connectivity compared to the remapping daughterboards.

For the majority of receivers, the rear transition modules just send all the input signals (with some initial conditioning) straight onto the motherboard. However, in the case of the electromagnetic barrel crates, the second type of transition module is used. This reroutes the highest eta signals (i.e. those furthest from the centre) back out onto connector E to be sent towards the summing patch panels. This is the only case where connector E is used (or even exists). Note that, being part of the transition module, connector E is also on the rear of the crate, rather than the front where output connectors A–D are located.

The consequence of this is that it was possible to manufacture identical remapping daughterboards for the electromagnetic and hadronic barrel region. In terms of the board type numbers, this means that 2 and 12 are equivalent. It was originally intended that 1 and 11 were identical, but a mistake in cabling meant that 11 had to be made to a different specification. In the cases of 1, 2 and 12, the remapping boards are tracked fully as the original specification for the tile case. The fact that this deals differently with the highest eta channel is irrelevant in the electromagnetic cases, since this signal never reaches the motherboard or daughterboard, having been removed by the rear transition module. Physically, the type number inscribed on the identical 2 and 12 boards is actually 2, rather than 12. However the specifications in Appendix B and the descriptions in this document still maintain type 12 as the overall effect of the receiver system from input to output is distinct in the two cases, and needs to be described.

6 Patch Panels

There are three distinct types of patch panels — the Tile calorimeter input patch panels (TCPP), the summing patch panels, and the receiver to PPM patch panels. For the first two cases, there is only one design. However, there are several different designs of receiver to PPM patch panels which deal with special cabling problems in four different regions, as described in the overview. Because the requirements are different at positive and negative eta, this means that, in general, different configurations are needed at each end. However, this is not a problem for the EM barrel/endcap merging, or for the FCAL patch panel, so 2*2+2 = 6 different types of patch panel are needed for the receiver to PPM cabling. These patch panels are documented here, but also more fully specified in a separate receiver to PPM patch panel document [11].

All the patch panels are documented in Appendix C. As noted in the last section, suitable receiver re-mappings are chosen in order to simplify the receiver to PPM patch panels as far as possible. The placement of these patch panels has been defined, and assignment to crates and slots in the rack layout is illustrated in Appendix D, along with the details of input and output cabling. The TCPP system consists of 64 TCPPs in 4 passive crates which are labelled A14, A23, C14 and C23 and fit into two racks — one per side of the detector. In this naming system, the letter A or C denotes the side, and the numbers stand for the quadrants dealt with by each crate, so crates A14 and A23 feed signals into receiver crate 7, and C14 and C23 feed receiver crate 8. The other patch panels are more diverse, but again fit into two racks, with each rack containing 3 passive crates to hold the different types of patch panel.

7 Preprocessor Crate Organisation

The PPM crates follow closely the organisation of the receiver crates described in section 4 and Appendix A. Again there are eight crates, but in this case they are numbered 0–7 for consistency with PPM crate geographical addressing. There is however an almost direct mapping between receiver and PPM crates, where PPM crate N processes, broadly speaking, the same signals as receiver crate N+1. The main area in which they differ is the distribution of the PPMs processing extreme eta and FCAL signals, and this difference also results in the fact that there are only 124 PPMs as opposed to 128 receiver modules. All of the FCAL signals, whether EM or hadronic, are processed in the hadronic PPM crates, which all have 16 modules. Of the electromagnetic crates, only the barrel ones contain 16 PPMs, the endcaps crates only needing 14 each. The details of module organisation within crates and analogue inputs and LVDS outputs are documented in Appendix E.

8 Processor Crates Organisation

There are four cluster processing crates filled with 14 CPMs each, and two jet/energy processing crates filled with 16 JEMs each. Each CPM crate handles signals from one phi quadrant, and the eta region dealt with by each CPM increases monotonically across the crate. These crates are labelled 0–3, with the obvious assignment that crate 0 processes quadrant 1, crate 1 processes quadrant 2 etc. The JEM crates process two phi quadrants each, since only 8 JEMs are required to process one quadrant. The modules are arranged in two groups of eight and again eta increases across the crate, with a logical (but not physical) gap in the middle. Crates are numbered 0 and 1, with crate 0 processing quadrants 1 and 3, and crate 1 processing 2 and 4. The processor modules receive their LVDS inputs on up to 24 connectors on the backplane — for the CPM only the first 20 are used. The crate organisation, and input cable assignment to each module is fully specified in Appendix F.

9 Other crates and cables

The bulk of the modules and cabling of the Level-1 Calorimeter Trigger system have been detailed in this document. This section briefly summarizes the missing items that are necessary to complete the system. Their connectivity is documented fully elsewhere [12].

There are three other crates in the system. Two are ROD crates which contain several ROD modules providing the readout of the trigger system. The other crate will contain all of the TTC interface to the central trigger system and the ROD Busy logic. Clearly the TTC crate needs to fanout TTC information to all the other modules in the system, and the RODs send back busy information to the Busy modules. The RODs themselves process information from all of the preprocessor and processor modules, and the link is provided by one or two high speed connections per (pre)processor module. All these links transfer data using the HP Glink protocol. Each ROD transfers reformatted data into the standard ATLAS DAQ data-flow environment via several Slink outputs.

Finally, each processor crate also contains merger modules which form the trigger bits which make up the final real–time output of the trigger system. To perform the final merging task, these modules require some inter–connectivity via cables which plug into the back of the modules onto the backplane. Some of them also have to be connected to the CTP to provide it with the calorimeter trigger bits to use for its level-1 decision.

A Receiver Crate module and cabling details

This appendix contains the full specification of the input and output cables to each of the receiver crates, as well as the ordering of modules within the eight crates. The remapping daughtercard identifiers (numbers from 1 to 22) are also detailed for each module. There is one figure for each crate, and the six figures dealing with the Liquid Argon receivers are essentially identical to those in figures 1, 2 and 6 of Bill's receiver cabling document [1]. The only difference of significance is the addition of the daughtercard number. The two Tile receivers are not documented elsewhere.

The tables show, for each slot in a receiver crate, which detector input cables should be plugged into the back of module (input cables 1–4) and the name of the cable outputs produced by the receiver after re-mapping (output connectors A–D on the front panel). Connector E is a special connector, only used for the EM barrel receivers, which comes from the rear transition module, unique to those barrel receivers, where signals to be summed are directed. The cable numbering schemes follow those laid out in the main text. To guide the eye, the tables are split into quadrant groupings, as labelled about halfway down the table. The final line gives the remapping daughtercard number required in the receiver module to perform the correct re-mapping for the slot and cables indicated.

Receiver crate 1: EM Barrel +Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	33A	35A	37A	39A	41A	43A	45A	47A	49A	51A	53A	55A	57A	59A	61A	63A
2	33B	35B	37B	39B	41B	43B	45B	47B	49B	51B	53B	55B	57B	59B	61B	63B
3	34A	36A	38A	40A	42A	44A	46A	48A	50A	52A	54A	56A	58A	60A	62A	64A
4	34B	36B	38B	40B	42B	44B	46B	48B	50B	52B	54B	56B	58B	60B	62B	64B
Connector	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
A	E08	E18	E28	E38	E48	E58	E68	E78	E88	E98	EA8	EB8	EC8	ED8	EE8	EF8
B	E09	E19	E29	E39	E49	E59	E69	E79	E89	E99	EA9	EB9	EC9	ED9	EE9	EF9
C	E0A	E1A	E2A	E3A	E4A	E5A	E6A	E7A	E8A	E9A	EAA	EBA	ECA	EDA	EEA	EFA
D	E0Bb	E1Bb	E2Bb	E3Bb	E4Bb	E5Bb	E6Bb	E7Bb	E8Bb	E9Bb	EABb	EBBb	ECBb	EDBb	EEBb	EFBb
E	E0Bs	E1Bs	E2Bs	E3Bs	E4Bs	E5Bs	E6Bs	E7Bs	E8Bs	E9Bs	EABs	EBBs	ECBs	EDBs	EEBs	EFBs
Interconnect	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2

Figure A.1: Receiver crate 1, inputs and outputs

Receiver crate 2: EM Barrel -Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	1A	3A	5A	7A	9A	11A	13A	15A	17A	19A	21A	23A	25A	27A	29A	31A
2	1B	3B	5B	7B	9B	11B	13B	15B	17B	19B	21B	23B	25B	27B	29B	31B
3	2A	4A	6A	8A	10A	12A	14A	16A	18A	20A	22A	24A	26A	28A	30A	32A
4	2B	4B	6B	8B	10B	12B	14B	16B	18B	20B	22B	24B	26B	28B	30B	32B
Connector	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
A	E04b	E14b	E24b	E34b	E44b	E54b	E64b	E74b	E84b	E94b	EA4b	EB4b	EC4b	ED4b	EE4b	EF4b
B	E05	E15	E25	E35	E45	E55	E65	E75	E85	E95	EA5	EB5	EC5	ED5	EE5	EF5
C	E06	E16	E26	E36	E46	E56	E66	E76	E86	E96	EA6	EB6	EC6	ED6	EE6	EF6
D	E07	E17	E27	E37	E47	E57	E67	E77	E87	E97	EA7	EB7	EC7	ED7	EE7	EF7
E	E04s	E14s	E24s	E34s	E44s	E54s	E64s	E74s	E84s	E94s	EA4s	EB4s	EC4s	ED4s	EE4s	EF4s
Interconnect	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure A.2: Receiver crate 2, inputs and outputs

Receiver crate 3: EM Endcap +Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	97A	93A	95A	98A	104A	100A	102A	105A	111A	107A	109A	112A	118A	114A	116A	119A
2	97B	93B	95B	98B	104B	100B	102B	105B	111B	107B	109B	112B	118B	114B	116B	119B
3	5S	94A	96A	99A	6S	101A	103A	106A	7S	108A	110A	113A	8S	115A	117A	120A
4		94B	96B	99B		101B	103B	106B		108B	110B	113B		115B	117B	120B
Connector	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
A	E0Be	E0C	E2C	E0Eo	E4Be	E4C	E6C	E4Eo	E8Be	E8C	EAC	E8Eo	ECBe	ECC	EEC	ECEo
B	E1Be	E0D	E2D	E0F	E5Be	E4D	E6D	E4F	E9Be	E8D	EAD	E8F	EDBe	ECD	EED	ECF
C	E2Be	E1C	E3C	E2Eo	E6Be	E5C	E7C	E6Eo	EABe	E9C	EBC	EAEo	EEBe	EDC	EFC	EEEo
D	E3Be	E1D	E3D	E2F	E7Be	E5D	E7D	E6F	EBBe	E9D	EBD	EAF	EFBe	EDD	EFD	EEF
E																
Interconnect	4	6	6	8	4	6	6	8	4	6	6	8	4	6	6	8

Figure A.3: Receiver crate 3, inputs and outputs

Receiver crate 4: EM Endcap -Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	69A	65A	67A	70A	76A	72A	74A	77A	83A	79A	81A	84A	90A	86A	88A	91A
2	69B	65B	67B	70B	76B	72B	74B	77B	83B	79B	81B	84B	90B	86B	88B	91B
3	1S	66A	68A	71A	2S	73A	75A	78A	3S	80A	82A	85A	4S	87A	89A	92A
4		66B	68B	71B		73B	75B	78B		80B	82B	85B		87B	89B	92B
Connector	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
A	E04e	E02	E22	E00	E44e	E42	E62	E40	E84e	E82	EA2	E80	EC4e	EC2	EE2	EC0
B	E14e	E03	E23	E01o	E54e	E43	E63	E41o	E94e	E83	EA3	E81o	ED4e	EC3	EE3	EC1o
C	E24e	E12	E32	E20	E64e	E52	E72	E60	EA4e	E92	EB2	EA0	EE4e	ED2	EF2	EE0
D	E34e	E13	E33	E21o	E74e	E53	E73	E61o	EB4e	E93	EB3	EA1o	EF4e	ED3	EF3	EE1o
E																
Interconnect	3	5	5	7	3	5	5	7	3	5	5	7	3	5	5	7

Figure A.4: Receiver crate 4, inputs and outputs

Receiver crate 5: Hadronic Endcap/FCAL +Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	129A	129B	129F	130D	131B	131F	132D	133B	133F	134D	135B	135F	136D	139A	139E	140C
2	131A	129C	130A	130E	131C	132A	132E	133C	134A	134E	135C	136A	136E	139C	139F	140D
3	133A	129D	130B	130F	131D	132B	132F	133D	134B	134F	135D	136B	136F	139D	140A	140E
4	135A	129E	130C		131E	132C		133E	134C		135E	136C		139B	140B	140F
Connector	Q1234	Quadrant 1			Quadrant 2			Quadrant 3			Quadrant 4			Q1234: FCAL 123		
A	H0Be	H0C	H0D	H0Eo	H4C	H4D	H4Eo	H8C	H8D	H8Eo	HCC	HCD	HCEo	E0G	H0Gx	H0Gy
B	H4Be	H1C	H1D	H0F	H5C	H5D	H4F	H9C	H9D	H8F	HDC	HDD	HCF	E4G	H4Gx	H4Gy
C	H8Be	H2C	H2D	H2Eo	H6C	H6D	H6Eo	HAC	HAD	HAEo	HEC	HED	HEEo	E8G	H8Gx	H8Gy
D	HCBe	H3C	H3D	H2F	H7C	H7D	H6F	HBC	HBD	HAF	HFC	HFD	HEF	ECG	HCGx	HCGy
E																
Interconnect	14	16	16	18	16	16	18	16	16	18	16	16	18	10	20	22

Figure A.5: Receiver crate 5, inputs and outputs

Receiver crate 6: Hadronic Endcap/FCAL -Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	121A	122D	121F	121B	124D	123F	123B	126D	125F	125B	128D	127F	127B	137A	137E	138C
2	123A	122E	122A	121C	124E	124A	123C	126E	126A	125C	128E	128A	127C	137B	137F	138D
3	125A	122F	122B	121D	124F	124B	123D	126F	126B	125D	128F	128B	127D	137C	138A	138E
4	127A		122C	121E		124C	123E		126C	125E		128C	127E	137D	138B	138F
Connector	Q1234	Quadrant 1			Quadrant 2			Quadrant 3			Quadrant 4			Q1234: FCAL 123		
A	H04e	H00	H02	H03	H40	H42	H43	H80	H82	H83	HC0	HC2	HC3	E0Z	H0Zx	H0Zy
B	H44e	H01o	H12	H13	H41o	H52	H53	H81o	H92	H93	HC1o	HD2	HD3	E4Z	H4Zx	H4Zy
C	H84e	H20	H22	H23	H60	H62	H63	HA0	HA2	HA3	HE0	HE2	HE3	E8Z	H8Zx	H8Zy
D	HC4e	H21o	H32	H33	H61o	H72	H73	HA1o	HB2	HB3	HE1o	HF2	HF3	ECZ	HCZx	HCZy
E																
Interconnect	13	17	15	15	17	15	15	17	15	15	17	15	15	9	19	21

Figure A.6: Receiver crate 6, inputs and outputs

Receiver crate 7: Hadronic Barrel (Tiles) +Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	A01	A05	A09	A13	A17	A21	A25	A29	A33	A37	A41	A45	A49	A53	A57	A61
2	A02	A06	A10	A14	A18	A22	A26	A30	A34	A38	A42	A46	A50	A54	A58	A62
3	A03	A07	A11	A15	A19	A23	A27	A31	A35	A39	A43	A47	A51	A55	A59	A63
4	A04	A08	A12	A16	A20	A24	A28	A32	A36	A40	A44	A48	A52	A56	A60	A64
Connector	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
A	H08	H18	H28	H38	H48	H58	H68	H78	H88	H98	HA8	HB8	HC8	HD8	HE8	HF8
B	H09	H19	H29	H39	H49	H59	H69	H79	H89	H99	HA9	HB9	HC9	HD9	HE9	HF9
C	H0A	H1A	H2A	H3A	H4A	H5A	H6A	H7A	H8A	H9A	HAA	HBA	HCA	HDA	HEA	HFA
D	H0Bb	H1Bb	H2Bb	H3Bb	H4Bb	H5Bb	H6Bb	H7Bb	H8Bb	H9Bb	HABb	HBBb	HCBb	HDBb	HEBb	HFBb
E																
Interconnect	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2

Figure A.7: Receiver crate 7, inputs and outputs

Receiver crate 8: Hadronic Barrel (Tiles) -Z

Input Cable	Slot Number															
	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	C01	C05	C09	C13	C17	C21	C25	C29	C33	C37	C41	C45	C49	C53	C57	C61
2	C02	C06	C10	C14	C18	C22	C26	C30	C34	C38	C42	C46	C50	C54	C58	C62
3	C03	C07	C11	C15	C19	C23	C27	C31	C35	C39	C43	C47	C51	C55	C59	C63
4	C04	C08	C12	C16	C20	C24	C28	C32	C36	C40	C44	C48	C52	C56	C60	C64
Connector	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
A	H04b	H14b	H24b	H34b	H44b	H54b	H64b	H74b	H84b	H94b	HA4b	HB4b	HC4b	HD4b	HE4b	HF4b
B	H05	H15	H25	H35	H45	H55	H65	H75	H85	H95	HA5	HB5	HC5	HD5	HE5	HF5
C	H06	H16	H26	H36	H46	H56	H66	H76	H86	H96	HA6	HB6	HC6	HD6	HE6	HF6
D	H07	H17	H27	H37	H47	H57	H67	H77	H87	H97	HA7	HB7	HC7	HD7	HE7	HF7
E																
Interconnect	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure A.8: Receiver crate 8, inputs and outputs

B Remapping Daughterboard specifications

This appendix contains the full specification of the connectivity needed in the 22 unique receiver module remapping configurations. It consists of 22 figures, the main feature of each figure being a standard table showing the mapping from input cable/pin numbers to output cable/pin numbers. In both cases, the 16 twisted pair signals are labelled as running from 1 to 16. Input cables are numbered 1 to 4, and output cables A to E, as in Bill's documents [1] and Appendix A. E is a smaller connector which is only used for the EM barrel to supply the inputs to the summing patch panels. It is located on special rear transition modules for receiver crates 1 and 2, which strip the relevant signals off before going to the main board. The x–axis represents the input pin numbers, and the y–axis the input cable numbers, and the table contents show the output pin numbers in the format Xnn, where X=A–E for output connector, and nn again runs from 1 to 16. If viewing the document in colour, output cables are also indicated by shading with a key given in figure B. Note that outputs that consist of summed signals appear twice in the table and are emphasized by being typed in ***bold italic***.

After the table comes a summary of the actual input/output cables and slot numbers in receiver crates for the relevant modules, including the quantity required. Finally, in order to illustrate where the re-ordering information comes from, there are rough sketches of the eta/phi region from the preprocessor and detector cable point of view. These show the pin numbering and input/output cables again using the colouring scheme shown in figure B.

Input Cables
Cable 1
Cable 2
Cable 3
Cable 4

Output Cables
Connector A
Connector B
Connector C
Connector D
Connector E

Figure B: Colouring key for remapping tables.

Note that these specifications should be a duplicate of those in another ATLAS note by Vittorio Paulone [13]. Also remapping board 2 has been produced to the specifications of 12, to reduce the number of designs needed. This is possible as the outputs to connector E are done via the unique EM barrel rear transition modules, rather than via the standard remapping daughtercard route.

1) Electromagnetic Barrel, negative eta

Input Cables / Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	phi
Cable 1	D10	D09	D14	D13	C10	C09	C14	C13	B10	B09	B14	B13	A10	A09	E03	n+1
Cable 2	D11	D12	D15	D16	C11	C12	C15	C16	B11	B12	B15	B16	A11	A12	E04	n+0
Cable 3	D06	D05	D02	D01	C06	C05	C02	C01	B06	B05	B02	B01	A06	A05	E01	n+3
Cable 4	D07	D08	D03	D04	C07	C08	C03	C04	B07	B08	B03	B04	A07	A08	E02	n+2
Output Cables	Connector D				Connector C				Connector B				Conn A		Conn E (Sum)	
eta	0.0				-0.4				-0.8				-1.2		-1.5	

Cable 1: TBB nA
Cable 2: TBB nB
Cable 3: TBB (n+1)A
Cable 4: TBB (n+1)B n = 1, 3, 5… 31

Connector A: Ex4b
Connector B: Ex5
Connector C: Ex6
Connector D: Ex7 x = 0 to F, ie 16 modules of this type required,
Connector E: Ex4s all placed in the EM barrel -ve eta receiver crate

Preprocessor View: increasing eta (increasing phi)

12 11	16 15	12 11	16 15	12 11	16 15	12 11
9 10	13 14	9 10	13 14	9 10	13 14	9 10
8 7	4 3	8 7	4 3	8 7	4 3	8 7
5 6	1 2	5 6	1 2	5 6	1 2	5 6

Detector View: increasing eta (increasing phi)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

Figure B.1: Remapping Daughterboard 1 — actually designed according to the original specification for daughterboard 11, with the E output implemented using a special RTM

2) Electromagnetic Barrel, positive eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	phi
	Cable 1	A16	A15	A12	A11	B16	B15	B12	B11	C16	C15	C12	C11	D16	D15	E01	n+0
	Cable 2	A13	A14	A09	A10	B13	B14	B09	B10	C13	C14	C09	C10	D13	D14	E02	n+1
	Cable 3	A04	A03	A08	A07	B04	B03	B08	B07	C04	C03	C08	C07	D04	D03	E03	n+2
	Cable 4	A01	A02	A05	A06	B01	B02	B05	B06	C01	C02	C05	C06	D01	D02	E04	n+3
	Output Cables	Connector A				Connector B				Connector C				Conn D		Conn E (Sum)	
	eta	0.0				0.4				0.8				1.2		1.5	

Cable 1: TBB nA
Cable 2: TBB nB
Cable 3: TBB (n+1)A
Cable 4: TBB (n+1)B n = 33, 35, 37… 63

Connector A: Ex8
Connector B: Ex9
Connector C: ExA
Connector D: ExBb x = 0 to F, ie 16 modules of this type required,
Connector E: ExBs all placed in the EM barrel +ve eta receiver crate

Preprocessor View: increasing eta; increasing phi

16	15	12	11	16	15	12	11	16	15	12	11	16	15
13	14	9	10	13	14	9	10	13	14	9	10	13	14
4	3	8	7	4	3	8	7	4	3	8	7	4	3
1	2	5	6	1	2	5	6	1	2	5	6	1	2

Detector View: increasing eta; increasing phi

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure B.2: Remapping Daughterboard 2 — actually designed according to the specification for daughterboard 12, with the E output implemented using a special RTM

3) Electromagnetic Barrel/Endcap C transition

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
	Cable 1	***D02***	***D03***	***D14***	***D15***	***C02***	***C03***	***C14***	***C15***	***B02***	***B03***	***B14***	***B15***	***A02***	***A03***	***A14***	***A15***	-1.5 to -1.4
	Cable 2	D01	D04	D13	D16	C01	C04	C13	C16	B01	B04	B13	B16	A01	A04	A13	A16	-1.6 to -1.5
	Cable 3	***D02***	***D03***	***D14***	***D15***	***C02***	***C03***	***C14***	***C15***	***B02***	***B03***	***B14***	***B15***	***A02***	***A03***	***A14***	***A15***	-1.5 to -1.4
	Cable 4																	
	Output Cables	Connector D				Connector C				Connector B				Connector A				
	phi	n				n+4				n+8				n+12			n+16	

Cable 1: TBB nA
Cable 2: TBB nB n = 69, 76, 83, 90
Cable 3: Sum m (mS) m = 1, 2, 3, 4
Cable 4:

Connector A: Ex4e
Connector B: E(x+1)4e
Connector C: E(x+2)4e x = 0, 4, 8, C, ie 4 modules of this type required,
Connector D: E(x+3)4e in slots 6, 10, 14, 18 of the electromagnetic endcap C receiver crate

Preprocessor View: increasing eta

16	Sum 15
13	Sum 14
4	Sum 3
1	Sum 2
16	Sum 15
13	Sum 14
4	Sum 3
1	Sum 2
16	Sum 15
13	Sum 14
4	Sum 3
1	Sum 2
16	Sum 15
13	Sum 14
4	Sum 3
1	Sum 2

increasing phi

Detector View: increasing eta

16	16	16
15	15	15
14	14	14
13	13	13
12	12	12
11	11	11
10	10	10
9	9	9
8	8	8
7	7	7
6	6	6
5	5	5
4	4	4
3	3	3
2	2	2
1	1	1

increasing phi

Figure B.3: Remapping Daughterboard 3

4) Electromagnetic Barrel/Endcap A transition

Input Cables	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
Cable 1	***A12***	***A09***	***A08***	***A05***	***B12***	***B09***	***B08***	***B05***	***C12***	***C09***	***C08***	***C05***	***D12***	***D09***	***D08***	***D05***	1.4 to 1.5
Cable 2	A11	A10	A07	A06	B11	B10	B07	B06	C11	C10	C07	C06	D11	D10	D07	D06	1.5 to 1.6
Cable 3	***A12***	***A09***	***A08***	***A05***	***B12***	***B09***	***B08***	***B05***	***C12***	***C09***	***C08***	***C05***	***D12***	***D09***	***D08***	***D05***	1.4 to 1.5
Cable 4																	
Output Cables	Connector A				Connector B				Connector C				Connector D				
phi	n				n+4				n+8				n+12				n+16

Cable 1: TBB nA
Cable 2: TBB nB n = 97, 104, 111, 118
Cable 3: Sum m (mS) m = 5, 6, 7, 8
Cable 4:

Connector A: ExBe
Connector B: E(x+1)Be
Connector C: E(x+2)Be x = 0, 4, 8, C, ie 4 modules of this type required,
Connector D: E(x+3)Be in slots 6, 10, 14, 18 of the electromagnetic endcap A receiver crate

Preprocessor View: increasing eta

Sum 12	11
Sum 9	10
Sum 8	7
Sum 5	6
Sum 12	11
Sum 9	10
Sum 8	7
Sum 5	6
Sum 12	11
Sum 9	10
Sum 8	7
Sum 5	6
Sum 12	11
Sum 9	10
Sum 8	7
Sum 5	6

increasing phi

Detector View: increasing eta

1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16

increasing phi

Figure B.4: Remapping Daughterboard 4

5) Electromagnetic Endcap C, medium eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	phi
	Cable 1	B06	B07	B05	B08	B02	B03	B01	B04	A06	A07	A05	A08	A02	A03	A01	A04	n+1/n+0
	Cable 2	B10	B11	B09	B12	B14	B15	B13	B16	A10	A11	A09	A12	A14	A15	A13	A16	n+3/n+2
	Cable 3	D06	D07	D05	D08	D02	D03	D01	D04	C06	C07	C05	C08	C02	C03	C01	C04	n+5/n+4
	Cable 4	D10	D11	D09	D12	D14	D15	D13	D16	C10	C11	C09	C12	C14	C15	C13	C16	n+7/n+6

Output Cables	Signals 1–8	Signals 9–16
	Connector B	Connector A
	Connector D	Connector C

eta: -1.6 -1.8 -2.0 -2.2 -2.4

Cable 1: TBB nA
Cable 2: TBB nB
Cable 3: TBB (n+1)A
Cable 4: TBB (n+1)B   n = 65, 67, 72, 74, 79, 81, 86, 88

Connector A: Ex2
Connector B: Ex3
Connector C: E(x+1)2   x = 0, 2, 4, 6, 8, A, C, E, ie 8 modules of this type required,
Connector D: E(x+1)3   in slots 7, 8, 11, 12, 15, 16, 19, 20 of the electromagnetic endcap C receiver crate

Preprocessor View: (increasing eta; increasing phi)

16	15	12	11	16	15	12	11
13	14	9	10	13	14	9	10
4	3	8	7	4	3	8	7
1	2	5	6	1	2	5	6
16	15	12	11	16	15	12	11
13	14	9	10	13	14	9	10
4	3	8	7	4	3	8	7
1	2	5	6	1	2	5	6

Detector View: (increasing eta; increasing phi)

16	14	12	10	8	6	4	2
15	13	11	9	7	5	3	1
16	14	12	10	8	6	4	2
15	13	11	9	7	5	3	1
16	14	12	10	8	6	4	2
15	13	11	9	7	5	3	1
16	14	12	10	8	6	4	2
15	13	11	9	7	5	3	1

Figure B.5: Remapping Daughterboard 5

6) Electromagnetic Endcap A, medium eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	phi
	Cable 1	A16	A13	A15	A14	A12	A09	A11	A10	B16	B13	B15	B14	B12	B09	B11	B10	n+0/n+1
	Cable 2	A04	A01	A03	A02	A08	A05	A07	A06	B04	B01	B03	B02	B08	B05	B07	B06	n+2/n+3
	Cable 3	C16	C13	C15	C14	C12	C09	C11	C10	D16	D13	D15	D14	D12	D09	D11	D10	n+4/n+5
	Cable 4	C04	C01	C03	C02	C08	C05	C07	C06	D04	D01	D03	D02	D08	D05	D07	D06	n+6/n+7

Output Cables	Signals 1–8	Signals 9–16
	Connector A	Connector B
	Connector C	Connector D

eta: 1.6 1.8 2.0 2.2 2.4

Cable 1: TBB nA
Cable 2: TBB nB
Cable 3: TBB (n+1)A
Cable 4: TBB (n+1)B n = 93, 95, 100, 102, 107, 109, 114, 116

Connector A: ExC
Connector B: ExD
Connector C: E(x+1)C x = 0, 2, 4, 6, 8, A, C, E, ie 8 modules of this type required,
Connector D: E(x+1)D in slots 7, 8, 11, 12, 15, 16, 19, 20 of the electromagnetic endcap A receiver crate

Preprocessor View: (increasing eta →, increasing phi ↓)

16	15	12	11	16	15	12	11
13	14	9	10	13	14	9	10
4	3	8	7	4	3	8	7
1	2	5	6	1	2	5	6
16	15	12	11	16	15	12	11
13	14	9	10	13	14	9	10
4	3	8	7	4	3	8	7
1	2	5	6	1	2	5	6

Detector View: (increasing eta →, increasing phi ↓)

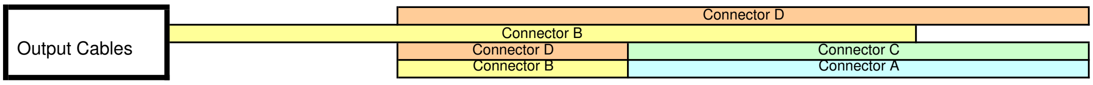
1	3	5	7	9	11	13	15
2	4	6	8	10	12	14	16
1	3	5	7	9	11	13	15
2	4	6	8	10	12	14	16
1	3	5	7	9	11	13	15
2	4	6	8	10	12	14	16
1	3	5	7	9	11	13	15
2	4	6	8	10	12	14	16

Figure B.6: Remapping Daughterboard 6

7) Electromagnetic Endcap C, extreme eta

Input Cables

Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1					D04	D16	D08	D12	D02	D03	D14	D15	D06	D07	D10	D11
Cable 2	B02	B03	B14	B15	B06	B07	B10	B11		B04	B16	B08	B12			
Cable 3					D01	D13	D05	D09	C03	C07	C11	C15	C04	C08	C12	C16
Cable 4					B01	B13	B05	B09	A03	A07	A11	A15	A04	A08	A12	A16

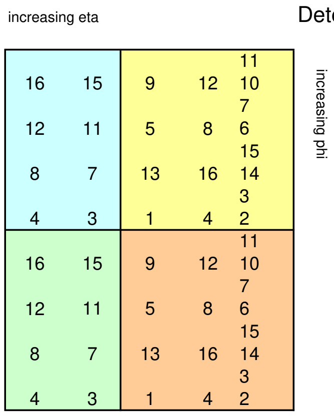


Cable 1: TBB nA
Cable 2: TBB nB
Cable 3: TBB (n+1)A
Cable 4: TBB (n+1)B n = 70, 77, 84, 91

Connector A: Ex0
Connector B: Ex1o
Connector C: E(x+2)0 x = 0, 4, 8, C, ie 4 modules of this type required,
Connector D: E(x+2)1o in slots 9, 13, 17, 21 of the electromagnetic endcap C receiver crate

Preprocessor View:

(ie signals to
PPM7 sparsifier)



Detector View:

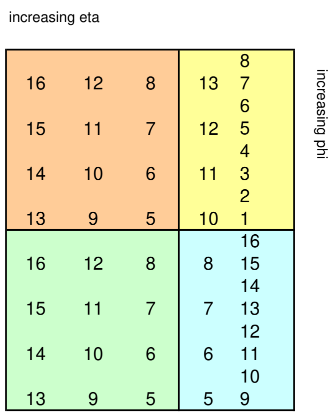
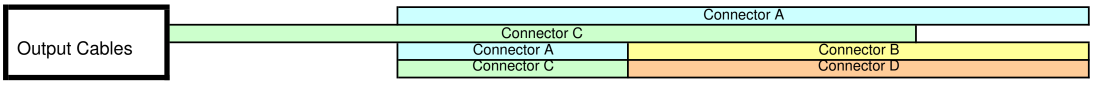


Figure B.7: Remapping Daughterboard 7

8) Electromagnetic Endcap A, extreme eta

Input Cables

Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1					A15	A03	A11	A07	A16	A13	A04	A01	A12	A09	A08	A05
Cable 2	C16	C13	C04	C01	C12	C09	C08	C05		C15	C03	C11	C07			
Cable 3					A14	A02	A10	A06	B16	B12	B08	B04	B15	B11	B07	B03
Cable 4					C14	C02	C10	C06	D16	D12	D08	D04	D15	D11	D07	D03



Cable 1: TBB nA
Cable 2: TBB nB
Cable 3: TBB (n+1)A
Cable 4: TBB (n+1)B n = 98,105,112,119

Connector A: ExEo
Connector B: ExF
Connector C: E(x+2)Eo x = 0, 4, 8, C, ie 4 modules of this type required,
Connector D: E(x+2)F in slots 9, 13, 17, 21 of the electromagnetic endcap A receiver crate

Preprocessor View: Detector View:

(ie signals to PPM7 sparsifier)

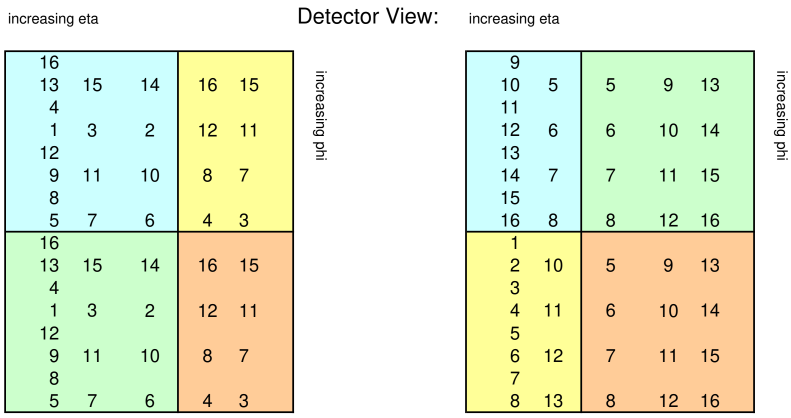


Figure B.8: Remapping Daughterboard 8

9) Forward Calorimeter, Endcap C, electromagnetic layer

Input Cables	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1	B01	B02	B05	B06	B03	B04	B07	B08	B09	B10	B13	B14	B11	B12	B15	B16
Cable 2	C01	C02	C05	C06	C03	C04	C07	C08	C09	C10	C13	C14	C11	C12	C15	C16
Cable 3	A01	A02	A05	A06	A03	A04	A07	A08	A09	A10	A13	A14	A11	A12	A15	A16
Cable 4	D01	D02	D05	D06	D03	D04	D07	D08	D09	D10	D13	D14	D11	D12	D15	D16

Output Cables	
	Connector B
	Connector C
	Connector A
	Connector D

Cable 1: TDB 137A
Cable 2: TDB 137B
Cable 3: TDB 137C
Cable 4: TDB 137D

Connector A: E0Z
Connector B: E4Z
Connector C: E8Z
Connector D: ECZ

One module of this type required, in slot 19 of hadronic endcap C receiver crate

Preprocessor View: increasing eta

16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1
16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1
16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1
16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1

increasing phi

Detector View: increasing eta

16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1
16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1
16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1
16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1

increasing phi

Figure B.9: Remapping Daughterboard 9

10) Forward Calorimeter, Endcap A, electromagnetic layer

Input Cables

Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1	A16	A15	A12	A11	A14	A13	A10	A09	A08	A07	A04	A03	A06	A05	A02	A01
Cable 2	B16	B15	B12	B11	B14	B13	B10	B09	B08	B07	B04	B03	B06	B05	B02	B01
Cable 3	C16	C15	C12	C11	C14	C13	C10	C09	C08	C07	C04	C03	C06	C05	C02	C01
Cable 4	D16	D15	D12	D11	D14	D13	D10	D09	D08	D07	D04	D03	D06	D05	D02	D01

Output Cables	
	Connector A
	Connector B
	Connector C
	Connector D

Cable 1:	TDB 139A
Cable 2:	TDB 139C
Cable 3:	TDB 139D
Cable 4:	TDB 139B

Connector A:	E0G
Connector B:	E4G
Connector C:	E8G
Connector D:	ECG

One module of this type required, in slot 19 of hadronic endcap A receiver crate

Preprocessor View: increasing eta, increasing phi

16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1
16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1
16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1
16	15	14	13
12	11	10	9
8	7	6	5
4	3	2	1

Detector View: increasing eta, increasing phi

1	2	5	6
3	4	7	8
9	10	13	14
11	12	15	16
1	2	5	6
3	4	7	8
9	10	13	14
11	12	15	16
1	2	5	6
3	4	7	8
9	10	13	14
11	12	15	16
1	2	5	6
3	4	7	8
9	10	13	14
11	12	15	16

Figure B.10: Remapping Daughterboard 10

11) Tile Calorimeter, negative eta

Input Cables	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	phi
Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	phi
Cable 1	D11	D12	D15	D16	C11	C12	C15	C16	B11	B12	B15	B16	A11	A12	A15	n+0
Cable 2	D10	D09	D14	D13	C10	C09	C14	C13	B10	B09	B14	B13	A10	A09	A14	n+1
Cable 3	D07	D08	D03	D04	C07	C08	C03	C04	B07	B08	B03	B04	A07	A08	A03	n+2
Cable 4	D06	D05	D02	D01	C06	C05	C02	C01	B06	B05	B02	B01	A06	A05	A02	n+3
Output Cables	Connector D				Connector C				Connector B				Connector A			
eta	0.0				-0.4				-0.8				-1.2		-1.5	

Cable 1: Tile cable Cn
Cable 2: Tile cable C(n+1)
Cable 3: Tile cable C(n+2)
Cable 4: Tile cable C(n+3) n = 1, 5, 9…61

Connector A: Hx4b
Connector B: Hx5
Connector C: Hx6 x = 0 to F, ie 16 modules of this type required,
Connector D: Hx7 all placed in the hadronic barrel -ve eta receiver crate

Preprocessor View: (increasing eta →, increasing phi)

15	12	11	16	15	12	11	16	15	12	11	16	15	12	11
14	9	10	13	14	9	10	13	14	9	10	13	14	9	10
3	8	7	4	3	8	7	4	3	8	7	4	3	8	7
2	5	6	1	2	5	6	1	2	5	6	1	2	5	6

Detector View: (increasing eta →, increasing phi)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Figure B.11: Remapping Daughterboard 11

12) Tile Calorimeter, positive eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	phi
	Cable 1	A16	A15	A12	A11	B16	B15	B12	B11	C16	C15	C12	C11	D16	D15	D12	n+0
	Cable 2	A13	A14	A09	A10	B13	B14	B09	B10	C13	C14	C09	C10	D13	D14	D09	n+1
	Cable 3	A04	A03	A08	A07	B04	B03	B08	B07	C04	C03	C08	C07	D04	D03	D08	n+2
	Cable 4	A01	A02	A05	A06	B01	B02	B05	B06	C01	C02	C05	C06	D01	D02	D05	n+3
	Output Cables	Connector A				Connector B				Connector C				Connector D			

eta 0.0 0.4 0.8 1.2 1.5

Cable 1: Tile cable An
Cable 2: Tile cable A(n+1)
Cable 3: Tile cable A(n+2)
Cable 4: Tile cable A(n+3) n = 1, 5, 9…61

Connector A: Hx8
Connector B: Hx9
Connector C: HxA x = 0 to F, ie 16 modules of this type required,
Connector D: HxBb all placed in the hadronic barrel +ve eta receiver crate

Preprocessor View:

increasing eta (columns), increasing phi (rows)

16 15 12 11	16 15 12 11	16 15 12 11	16 15 12
13 14 9 10	13 14 9 10	13 14 9 10	13 14 9
4 3 8 7	4 3 8 7	4 3 8 7	4 3 8
1 2 5 6	1 2 5 6	1 2 5 6	1 2 5

Detector View:

increasing eta (columns), increasing phi (rows)

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Figure B.12: Remapping Daughterboard 12 — physically labelled as type 2 as that daughterboard was designed to be identical

13) Hadronic Endcap to Tile transition, Endcap C

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
	Cable 1	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	-1.6 to -1.5
	Cable 2	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	
	Cable 3	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	
	Cable 4	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	

Output Cables: Connector A, Connector B, Connector C, Connector D

phi: n, n+4, n+8, n+12, n+16

Cable 1: TDB 121A
Cable 2: TDB 123A
Cable 3: TDB 125A
Cable 4: TDB 127A

Connector A: H04e
Connector B: H44e
Connector C: H84e
Connector D: HC4e

One module of this type required, in slot 6 of hadronic endcap C receiver crate (crate 6)

Preprocessor View: increasing phi (+16); increasing phi (+1)

1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16

Detector View: increasing phi (+16); increasing phi (+1)

16	16	16	16
15	15	15	15
14	14	14	14
13	13	13	13
12	12	12	12
11	11	11	11
10	10	10	10
9	9	9	9
8	8	8	8
7	7	7	7
6	6	6	6
5	5	5	5
4	4	4	4
3	3	3	3
2	2	2	2
1	1	1	1

Figure B.13: Remapping Daughterboard 13

14) Hadronic Endcap to Tile transition, Endcap A

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
	Cable 1	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	
	Cable 2	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16	1.5 to 1.6
	Cable 3	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15	C16	
	Cable 4	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	D11	D12	D13	D14	D15	D16	

Output Cables	
	Connector A
	Connector B
	Connector C
	Connector D

phi	n	n+4	n+8	n+12	n+16

Cable 1: TDB 129A
Cable 2: TDB 131A
Cable 3: TDB 133A
Cable 4: TDB 135A

Connector A: H0Be
Connector B: H4Be
Connector C: H8Be
Connector D: HCBe

One module of this type required, in slot 6 of hadronic endcap A receiver crate (crate 5)

Preprocessor View: increasing phi (+16)

1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16

increasing phi (+1)

Detector View: increasing phi (+16)

1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16

increasing phi (+1)

Figure B.14: Remapping Daughterboard 14

15) Hadronic Endcap C, medium eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
																		-1.6/-2.0
	Cable 1	D06	D07	D10	D11	C06	C07	C10	C11	B06	B07	B10	B11	A06	A07	A10	A11	-1.7/-2.1
	Cable 2	D05	D08	D09	D12	C05	C08	C09	C12	B05	B08	B09	B12	A05	A08	A09	A12	-1.8/-2.2
	Cable 3	D02	D03	D14	D15	C02	C03	C14	C15	B02	B03	B14	B15	A02	A03	A14	A15	-1.9/-2.3
	Cable 4	D01	D04	D13	D16	C01	C04	C13	C16	B01	B04	B13	B16	A01	A04	A13	A16	-2.0/-2.4
	Output Cables	Connector D				Connector C				Connector B				Connector A				
	phi	n				n+4				n+8				n+12				n+16

Cable 1:	TDB nB	or	nF	
Cable 2:	TDB nC	or	(n+1)A	
Cable 3:	TDB nD	or	(n+1)B	
Cable 4:	TDB nE	or	(n+1)C	n = 121, 123, 125, 127

Connector A:	Hx3	or	Hx2	x = 0, 4, 8, C, ie 4*2=8 modules of this type required, in
Connector B:	H(x+1)3	or	H(x+1)2	slots 8, 9, 11, 12, 14, 15, 17, 18 of hadronic endcap C receiver crate
Connector C:	H(x+2)3	or	H(x+2)2	slots 8, 11, 14, 17 have eta -2.4 to -2.0 (Hx2) modules
Connector D:	H(x+3)3	or	H(x+3)2	slots 9, 12, 15, 18 have eta -2.0 to -1.6 (Hx3) modules

Preprocessor View: increasing eta (→), increasing phi (↓)

16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6
16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6
16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6
16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6

Detector View: increasing eta (→), increasing phi (↓)

16	16	16	16
15	15	15	15
14	14	14	14
13	13	13	13
12	12	12	12
11	11	11	11
10	10	10	10
9	9	9	9
8	8	8	8
7	7	7	7
6	6	6	6
5	5	5	5
4	4	4	4
3	3	3	3
2	2	2	2
1	1	1	1

Figure B.15: Remapping Daughterboard 15

16) Hadronic Endcap A, medium eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta 1.6/2.0
	Cable 1	A16	A13	A04	A01	B16	B13	B04	B01	C16	C13	C04	C01	D16	D13	D04	D01	1.7/2.1
	Cable 2	A15	A14	A03	A02	B15	B14	B03	B02	C15	C14	C03	C02	D15	D14	D03	D02	1.8/2.2
	Cable 3	A12	A09	A08	A05	B12	B09	B08	B05	C12	C09	C08	C05	D12	D09	D08	D05	1.9/2.3
	Cable 4	A11	A10	A07	A06	B11	B10	B07	B06	C11	C10	C07	C06	D11	D10	D07	D06	2.0/2.4
	Output Cables	Connector A				Connector B				Connector C				Connector D				
	phi	n			n+4				n+8				n+12				n+16	

Cable 1:	TDB nB	or	nF	
Cable 2:	TDB nC	or	(n+1)A	
Cable 3:	TDB nD	or	(n+1)B	
Cable 4:	TDB nE	or	(n+1)C	n = 129, 131, 133, 135

Connector A:	HxC	or	HxD	x = 0, 4, 8, C, ie 4*2=8 modules of this type required, in
Connector B:	H(x+1)C	or	H(x+1)D	slots 7, 8, 10, 11, 13, 14, 16, 17 of hadronic endcap A receiver crate
Connector C:	H(x+2)C	or	H(x+2)D	slots 7, 10, 13, 16 have eta 1.6 to 2.0 (HxC) modules
Connector D:	H(x+3)C	or	H(x+3)D	slots 8, 11, 14, 17 have eta 2.0 to 2.4 (HxD) modules

Preprocessor View: increasing eta

16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6
16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6
16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6
16	15	12	11
13	14	9	10
4	3	8	7
1	2	5	6

increasing phi

Detector View: increasing eta

1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16

increasing phi

Figure B.16: Remapping Daughterboard 16

17) Hadronic Endcap C, extreme eta

Input Cables	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta
Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	-2.4
Cable 1	D02	D03	D14	D15	D06	D07	D10	D11	B02	B03	B14	B15	B06	B07	B10	B11	-2.5
Cable 2	D04	D16	D08	D12	B04	B16	B08	B12	D01	D13	D05	D09	B01	B13	B05	B09	-2.7/2.9
Cable 3	C03	C07	C11	C15	A03	A07	A11	A15	C04	C08	C12	C16	A04	A08	A12	A16	-3.1/-3.2
Cable 4																	

Output Cables	Signals 1–4	Signals 5–8	Signals 9–12	Signals 13–16
	Connector D	Connector D / Connector B	Connector B / Connector D	Connector B
	Connector C	Connector A	Connector C	Connector A

Cable 1: TDB nD
Cable 2: TDB nE
Cable 3: TDB nF n = 122, 124, 126, 128
Cable 4:

Connector A: Hx0
Connector B: Hx1o
Connector C: H(x+2)0 x = 0, 4, 8, C, ie 4 modules of this type required,
Connector D: H(x+2)1o in slots 7, 10, 13, 16 of the hadronic endcap C receiver crate

Preprocessor View: increasing eta

(ie signals to PPM7 sparsifier)

increasing phi

				11
16	15	9	12	10
				7
12	11	5	8	6
				15
8	7	13	16	14
				3
4	3	1	4	2
				11
16	15	9	12	10
				7
12	11	5	8	6
				15
8	7	13	16	14
				3
4	3	1	4	2

Detector View: increasing eta

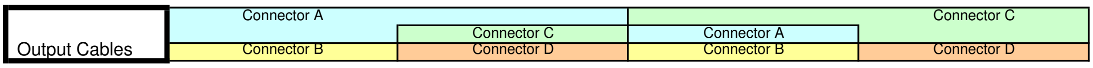
increasing phi

				16
16	8	16	8	15
				14
15	7	15	7	13
				12
14	6	14	6	11
				10
13	5	13	5	9
				8
12	4	12	4	7
				6
11	3	11	3	5
				4
10	2	10	2	3
				2
9	1	9	1	1

Figure B.17: Remapping Daughterboard 17

18) Hadronic Endcap A, extreme eta

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	eta 2.4
	Cable 1	A16	A13	A04	A01	A12	A09	A08	A05	C16	C13	C04	C01	C12	C09	C08	C05	2.5
	Cable 2	A15	A03	A11	A07	C15	C03	C11	C07	A14	A02	A10	A06	C14	C02	C10	C06	2.7/2.9
	Cable 3	B16	B12	B08	B04	D16	D12	D08	D04	B15	B11	B07	B03	D15	D11	D07	D03	3.1/3.2
	Cable 4																	

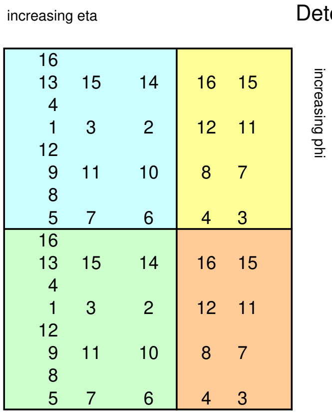


Cable 1: TDB nD
Cable 2: TDB nE
Cable 3: TDB nF n = 130, 132, 134, 136
Cable 4:

Connector A: HxEo
Connector B: HxF
Connector C: H(x+2)Eo x = 0, 4, 8, C, ie 4 modules of this type required,
Connector D: H(x+2)F in slots 9, 12, 15, 18 of the hadronic endcap A receiver crate

Preprocessor View:

(ie signals to PPM7 sparsifier)



Detector View:

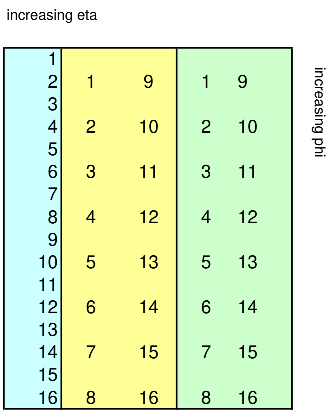


Figure B.18: Remapping Daughterboard 18

19) Forward Calorimeter, Endcap C, first hadronic layer

Input Cables: Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1	***B06***	***B06***	***B02***	***B02***	***B08***	***B08***	***B04***	***B04***	***B14***	***B14***	***B10***	***B10***	***B16***	***B16***	***B12***	***B12***
Cable 2	***A06***	***A06***	***A02***	***A02***	***A08***	***A08***	***A04***	***A04***	***A14***	***A14***	***A10***	***A10***	***A16***	***A16***	***A12***	***A12***
Cable 3	***D06***	***D06***	***D02***	***D02***	***D08***	***D08***	***D04***	***D04***	***D14***	***D14***	***D10***	***D10***	***D16***	***D16***	***D12***	***D12***
Cable 4	***C06***	***C06***	***C02***	***C02***	***C08***	***C08***	***C04***	***C04***	***C14***	***C14***	***C10***	***C10***	***C16***	***C16***	***C12***	***C12***

Output Cables	
	Connector B
	Connector A
	Connector D
	Connector C

Cable 1: TDB 137E
Cable 2: TDB 137F
Cable 3: TDB 138A
Cable 4: TDB 138B

Connector A: H0Zx
Connector B: H4Zx
Connector C: H8Zx
Connector D: HCZx

One module of this type required, in slot 20 of hadronic endcap C receiver crate

Preprocessor View: (increasing eta →; increasing phi ↓)

Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2

Detector View: (increasing eta →; increasing phi ↓)

13	14	9	10
15	16	11	12
5	6	1	2
7	8	3	4
13	14	9	10
15	16	11	12
5	6	1	2
7	8	3	4
13	14	9	10
15	16	11	12
5	6	1	2
7	8	3	4
13	14	9	10
15	16	11	12
5	6	1	2
7	8	3	4

Figure B.19: Remapping Daughterboard 19

20) Forward Calorimeter, Endcap A, first hadronic layer

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	Cable 1	A12	A12	A16	A16	A10	A10	A14	A14	A04	A04	A08	A08	A02	A02	A06	A06
	Cable 2	B12	B12	B16	B16	B10	B10	B14	B14	B04	B04	B08	B08	B02	B02	B06	B06
	Cable 3	C12	C12	C16	C16	C10	C10	C14	C14	C04	C04	C08	C08	C02	C02	C06	C06
	Cable 4	D12	D12	D16	D16	D10	D10	D14	D14	D04	D04	D08	D08	D02	D02	D06	D06

Output Cables	
	Connector A
	Connector B
	Connector C
	Connector D

Cable 1: TDB 139E
Cable 2: TDB 139F
Cable 3: TDB 140A
Cable 4: TDB 140B

Connector A: H0Gx
Connector B: H4Gx
Connector C: H8Gx
Connector D: HCGx

One module of this type required, in slot 20 of hadronic endcap A receiver crate

Preprocessor View: increasing eta; increasing phi

Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2

Detector View: increasing eta; increasing phi

4	3	8	7
2	1	6	5
12	11	16	15
10	9	14	13
4	3	8	7
2	1	6	5
12	11	16	15
10	9	14	13
4	3	8	7
2	1	6	5
12	11	16	15
10	9	14	13
4	3	8	7
2	1	6	5
12	11	16	15
10	9	14	13

Figure B.20: Remapping Daughterboard 20

21) Forward Calorimeter, Endcap C, second hadronic layer

Input Cables

Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1	***B04***	***B04***	***B08***	***B08***	***B02***	***B02***	***B06***	***B06***	***B12***	***B12***	***B16***	***B16***	***B10***	***B10***	***B14***	***B14***
Cable 2	***A04***	***A04***	***A08***	***A08***	***A02***	***A02***	***A06***	***A06***	***A12***	***A12***	***A16***	***A16***	***A10***	***A10***	***A14***	***A14***
Cable 3	***D04***	***D04***	***D08***	***D08***	***D02***	***D02***	***D06***	***D06***	***D12***	***D12***	***D16***	***D16***	***D10***	***D10***	***D14***	***D14***
Cable 4	***C04***	***C04***	***C08***	***C08***	***C02***	***C02***	***C06***	***C06***	***C12***	***C12***	***C16***	***C16***	***C10***	***C10***	***C14***	***C14***

Output Cables	
	Connector B
	Connector A
	Connector D
	Connector C

Cable 1: TDB 138C
Cable 2: TDB 138D
Cable 3: TDB 138E
Cable 4: TDB 138F

Connector A: H0Zy
Connector B: H4Zy
Connector C: H8Zy
Connector D: HCZy

One module of this type required, in slot 20 of hadronic endcap C receiver crate

Preprocessor View: increasing eta, increasing phi

Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2

Detector View: increasing eta, increasing phi

11	12	15	16
9	10	13	14
3	4	7	8
1	2	5	6
11	12	15	16
9	10	13	14
3	4	7	8
1	2	5	6
11	12	15	16
9	10	13	14
3	4	7	8
1	2	5	6
11	12	15	16
9	10	13	14
3	4	7	8
1	2	5	6

Figure B.21: Remapping Daughterboard 21

22) Forward Calorimeter, Endcap A, second hadronic layer

Input Cables / Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1	***A02***	***A02***	***A06***	***A06***	***A04***	***A04***	***A08***	***A08***	***A10***	***A10***	***A14***	***A14***	***A12***	***A12***	***A16***	***A16***
Cable 2	***B02***	***B02***	***B06***	***B06***	***B04***	***B04***	***B08***	***B08***	***B10***	***B10***	***B14***	***B14***	***B12***	***B12***	***B16***	***B16***
Cable 3	***C02***	***C02***	***C06***	***C06***	***C04***	***C04***	***C08***	***C08***	***C10***	***C10***	***C14***	***C14***	***C12***	***C12***	***C16***	***C16***
Cable 4	***D02***	***D02***	***D06***	***D06***	***D04***	***D04***	***D08***	***D08***	***D10***	***D10***	***D14***	***D14***	***D12***	***D12***	***D16***	***D16***

Output Cables
Connector A
Connector B
Connector C
Connector D

Cable 1: TDB 140C
Cable 2: TDB 140D
Cable 3: TDB 140E
Cable 4: TDB 140F

Connector A: H0Gy
Connector B: H4Gy
Connector C: H8Gy
Connector D: HCGy

One module of this type required, in slot 21 of hadronic endcap A receiver crate

Preprocessor View: increasing eta, increasing phi

Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2
Sum 16	Sum 14
Sum 12	Sum 10
Sum 8	Sum 6
Sum 4	Sum 2

Detector View: increasing eta, increasing phi

16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1
16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1
16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1
16	15	12	11
14	13	10	9
8	7	4	3
6	5	2	1

Figure B.22: Remapping Daughterboard 22

C Patch Panel specifications

This appendix contains the full specifications for the connectivity of all the patch panels required — that means the patch panels before the receivers, between receivers and the large number of types of patch panels for the receiver outputs. The main feature of each figure is a table similar to those in Appendix B. These again show the mapping from input cable/pin numbers to output cable/pin numbers. All the patch panels are passive and simply provide a repackaging of the signals. In most cases the input and output cables consist of 16 twisted pair signals, which are labelled as running from 1 to 16. For the summing patch panel inputs, the cables only have 4 twisted pairs, numbered 1–4. As before, the input pin numbers form the x–axis, and the cable number the y–axis, and the contents show the output pin number in the format Xnn (X can be A–D for the output connector). Output cables are also indicated by shading with the same convention as in Appendix B and illustrated in figure B.

The input cables for the Tile Calorimeter Patch Panels (TCPP) are actually of a different type to most of the analogue signals cables. The connector is not the standard Sub D 37c, but have 50 pins. The pin assignment is detailed in section 3.1, and the numbers in the patch panel specification should be read as the 'reference number' in the table. Note that there are also individual lemo outputs on the patch panels for the crack signals. These are not currently foreseen to be sent to the calorimeter or the muon trigger systems.

The number of input and output cables varies between patch panels. The majority are of a relatively simple 2:1 merging or 1:2 sparsification topology. There is one case of 4:1 merging (the summing patch panels) and the most complex region is the Tile to HEC merging, which has 5 input cables merged to produce 4 outputs.

After the table comes a summary of the names of the actual input and output cables involved in each type of patch panel, and some information about their multiplicity. The scheme of patch panels described here are consistent with the choice of 22 types of remapping daughterboards. At the cost of increasing the complexity of the patch panels, it may be possible to reduce the number different types of these daughterboards that are required.

Note that the designs in figures C.3 and C.4 are actually identical, and so only one type of patch panel is needed. The two specifications are separated for historical reasons.

Tile input cable merging (TCPP)

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	Cable 1	A09	A08	A07	A06	A05	A04	A03	A02	A01	B07	B06	B05	B04	B03	B02	B01
	Cable 2	A15	A14	A13	A12	A11	A10	L #1			B11	B10	B09	B08	L #2		

Input Cable 1:	LBPn	LB = long barrel
Input Cable 2:	EBPn	EB = extended barrel
Output Cable A:	Pn	P = A or C, n = 1-64, ie 128 needed in total
Output Cable B:	Pnm	naming as above, 128 muon cables
Lemo Outputs:		Gap/Crack signals L#1 and L#2 go nowhere for now

Figure C.1: Patch panel for Tile input cables

Summing Patch Panels

Input Cables	Signal Number	1	2	3	4
	Cable 1	A01	A02	A03	A04
	Cable 2	A05	A06	A07	A08
	Cable 3	A09	A10	A11	A12
	Cable 4	A13	A14	A15	A16

Input Cable 1:	E(x+3)4s	or	ExBs	
Input Cable 2:	E(x+2)4s	or	E(x+1)Bs	
Input Cable 3:	E(x+1)4s	or	E(x+2)Bs	
Input Cable 4:	Ex4s	or	E(x+3)Bs	x = 0, 4, 8, C
Output Cable A:	1S, 2S, 3S, 4S	or	5S, 6S, 7S, 8S	

Figure C.2: Summing Patch Panels

EM negative eta barrel/endcap merging

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	Cable 1	A01	A02	A03	A04									A13	A14	A15	A16
	Cable 2					A05	A06	A07	A08	A09	A10	A11	A12				

Input Cable 1: Ex4e
Input Cable 2: Ex4b

Output Cable A: Ex4 x = 0-F (ie four needed per quadrant)

Figure C.3: Patch panel for receiver outputs for PPM_4 electromagnetic at negative eta

EM positive eta barrel/endcap merging

Input Cables	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	Cable 1	A01	A02	A03	A04									A13	A14	A15	A16
	Cable 2					A05	A06	A07	A08	A09	A10	A11	A12				

Input Cable 1: ExBb
Input Cable 2: ExBe

Output Cable A: ExB x = 0-F (ie four needed per quadrant)

Figure C.4: Patch panel for receiver outputs for PPM_4 electromagnetic at positive eta

EM/Hadronic negative eta endcap sparsification

Input	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	Cable 1	B04	B06	B07	B08	A04	A06	A07	A08	A16	A10	A11	A12	B16	B10	B11	B12

Electromagnetic -Z rack

Input Cable 1: Ex1o

Output Cable A: Ex1
Output Cable B: E(x+1)1 x = 0, 2, 4, 6, 8, A, C, E (ie two needed per quadrant)

Hadronic -Z rack

Input Cable 1: Hx1o

Output Cable A: Hx1
Output Cable B: H(x+1)1 x = 0, 2, 4, 6, 8, A, C, E (ie two needed per quadrant)

Figure C.5: Patch panel for receiver outputs for PPM_7 at negative eta

EM/Hadronic positive eta endcap sparsification

Input	Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	Cable 1	A01	A08	A03	A04	B01	B08	B03	B04	B13	B12	B15	B16	A13	A12	A15	A16

Electromagnetic +Z rack

Input Cable 1: ExEo

Output Cable A: ExE
Output Cable B: E(x+1)E x = 0, 2, 4, 6, 8, A, C, E (ie two needed per quadrant)

Hadronic +Z rack

Input Cable 1: HxEo

Output Cable A: HxE
Output Cable B: H(x+1)E x = 0, 2, 4, 6, 8, A, C, E (ie two needed per quadrant)

Figure C.6: Patch panel for receiver outputs for PPM_7 at positive eta

Hadronic negative eta tile/endcap merging

Input Cables: Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1		A02	A03		A05	A06	A07	A08	A09	A10	A11	A12		A14	A15	
Cable 2		B02	B03		B05	B06	B07	B08	B09	B10	B11	B12		B14	B15	
Cable 3		C02	C03		C05	C06	C07	C08	C09	C10	C11	C12		C14	C15	
Cable 4		D02	D03		D05	D06	D07	D08	D09	D10	D11	D12		D14	D15	
Cable 5	A16	A13	A04	A01	B16	B13	B04	B01	C16	C13	C04	C01	D16	D13	D04	D01

Input Cable 1:	H04b	or	H44b	or	H84b	or	HC4b
Input Cable 2:	H14b	or	H54b	or	H94b	or	HD4b
Input Cable 3:	H24b	or	H64b	or	HA4b	or	HE4b
Input Cable 4:	H34b	or	H74b	or	HB4b	or	HF4b
Input Cable 5:	H04e	or	H44e	or	H84e	or	HC4e

Output Cable A:	H04	or	H44	or	H84	or	HC4
Output Cable B:	H14	or	H54	or	H94	or	HD4
Output Cable C:	H24	or	H64	or	HA4	or	HE4
Output Cable D:	H34	or	H74	or	HB4	or	HF4

Figure C.7: Patch panel for receiver outputs for PPM_4 hadronic at negative eta

Hadronic positive eta tile/endcap merging

Input Cables / Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1	A01	A02	A03	A04	A05			A08	A09			A12	A13	A14	A15	A16
Cable 2	B01	B02	B03	B04	B05			B08	B09			B12	B13	B14	B15	B16
Cable 3	C01	C02	C03	C04	C05			C08	C09			C12	C13	C14	C15	C16
Cable 4	D01	D02	D03	D04	D05			D08	D09			D12	D13	D14	D15	D16
Cable 5	A11	A10	A07	A06	B11	B10	B07	B06	C11	C10	C07	C06	D11	D10	D07	D06

Input Cable 1:	H0Bb	or	H4Bb	or	H8Bb	or	HCBb
Input Cable 2:	H1Bb	or	H5Bb	or	H9Bb	or	HDBb
Input Cable 3:	H2Bb	or	H6Bb	or	HABb	or	HEBb
Input Cable 4:	H3Bb	or	H7Bb	or	HBBb	or	HFBb
Input Cable 5:	H0Be	or	H4Be	or	H8Be	or	HCBe
Output Cable A:	H0B	or	H4B	or	H8B	or	HCB
Output Cable B:	H1B	or	H5B	or	H9B	or	HDB
Output Cable C:	H2B	or	H6B	or	HAB	or	HEB
Output Cable D:	H3B	or	H7B	or	HBB	or	HFB

Figure C.8: Patch panel for receiver outputs for PPM_4 hadronic at positive eta

FCAL hadronic merging (both ends)

Input Cables / Signal Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cable 1		A02		A04		A06		A08		A10		A12		A14		A16
Cable 2		A01		A03		A05		A07		A09		A11		A13		A15

Input Cable 1:	HnGx	or	HnZx	
Input Cable 2:	HnGy	or	HnZy	
Output Cable A:	HnG	or	HnZ	n = 0, 4, 8, C

Figure C.9: Patch panel for receiver outputs for PPM_9 hadronic at both ends

D Patch Panel crate and cabling details

This appendix details the placement and cabling of the TileCal Patch Panels (TCPP) and the Receiver to PPM Patch Panels. The figures in this appendix are composed of tables with the horizontal axis corresponding to the crate slot numbers as seen from the front of the crate - these slot numbers are also explicitly numbered in the first row of each table. The vertical axis specifies the input/output cable slots, and the contents show the name of the cable connected in each slot, from top to bottom.

For the TCPP system, there are 64 modules arranged in 4 crates of similar density to the receiver and PPM crates, and the arrangement of these crates is shown in the first four figures. The four input slots (in 1–4) are populated with the 50 pin connectors on the end of the long analogue cables from the detector, and are located on the back panel of the TCPP and thus also at the back of the crate. The output slots (out 1–4) are at the front and are filled with short cables with the standard 37 pin connector which go into receiver crates 7 and 8. Quadrant numbers are also shown — note the one slot gap between quadrants, as only 8 TCPPs are needed per quadrant at each end of the detector. The placement of crates follows from latency considerations. Firstly the two sides (A and C) of the detector are separated into two racks which are placed as close as possible to the corresponding receiver crates. Secondly, the quadrant allocation is made such that those with the longest cables (Quadrants 1 and 4) are in the bottom of the crate, to try to shorten necessary connections. The crate names come from the area of the detector processed, thus A or C for side, and 14 or 23 for quadrants.

For the receiver to PPM patch panels, there are 80 modules, of different types, arranged in 6 crates — three per side of the detector. The crates are named C0, C1, C2, A0, A1 and A2. The details of the connectivity of each type can be derived from the figures in Appendix C, but are also given in detail in a separate document [11]. The final two figures show the layout of the racks of these patch panel crates. Along with the names of the input and output cables, the type of patch panel needed in that slot is numbered. These numbers correspond to the scheme given in the detailed patch panel specification [11].

Slot	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Quadrant 2 (back panel)									Quadrant 3 (back panel)							
in(R) 1	EBC17	EBC19	EBC21	EBC23	EBC25	EBC27	EBC29	EBC31		EBC33	EBC35	EBC37	EBC39	EBC41	EBC43	EBC45	EBC47
in(R) 2	LBC17	LBC19	LBC21	LBC23	LBC25	LBC27	LBC29	LBC31		LBC33	LBC35	LBC37	LBC39	LBC41	LBC43	LBC45	LBC47
in(R) 3	EBC18	EBC20	EBC22	EBC24	EBC26	EBC28	EBC30	EBC32		EBC34	EBC36	EBC38	EBC40	EBC42	EBC44	EBC46	EBC48
in(R) 4	LBC18	LBC20	LBC22	LBC24	LBC26	LBC28	LBC30	LBC32		LBC34	LBC36	LBC38	LBC40	LBC42	LBC44	LBC46	LBC48
	Quadrant 2 (front panel)									Quadrant 3 (front panel)							
out(F) 1	C17	C19	C21	C23	C25	C27	C29	C31		C33	C35	C37	C39	C41	C43	C45	C47
out(F) 2	C17m	C19m	C21m	C23m	C25m	C27m	C29m	C31m		C33m	C35m	C37m	C39m	C41m	C43m	C45m	C47m
out(F) 3	C18	C20	C22	C24	C26	C28	C30	C32		C34	C36	C38	C40	C42	C44	C46	C48
out(F) 4	C18m	C20m	C22m	C24m	C26m	C28m	C30m	C32m		C34m	C36m	C38m	C40m	C42m	C44m	C46m	C48m

Figure D.1: TileCal patch panel crate C23 inputs and outputs

Slot	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Quadrant 1 (back panel)									Quadrant 4 (back panel)							
in(R) 1	EBC01	EBC03	EBC05	EBC07	EBC09	EBC11	EBC13	EBC15		EBC49	EBC51	EBC53	EBC55	EBC57	EBC59	EBC61	EBC63
in(R) 2	LBC01	LBC03	LBC05	LBC07	LBC09	LBC11	LBC13	LBC15		LBC49	LBC51	LBC53	LBC55	LBC57	LBC59	LBC61	LBC63
in(R) 3	EBC02	EBC04	EBC06	EBC08	EBC10	EBC12	EBC14	EBC16		EBC50	EBC52	EBC54	EBC56	EBC58	EBC60	EBC62	EBC64
in(R) 4	LBC02	LBC04	LBC06	LBC08	LBC10	LBC12	LBC14	LBC16		LBC50	LBC52	LBC54	LBC56	LBC58	LBC60	LBC62	LBC64
	Quadrant 1 (front panel)									Quadrant 4 (front panel)							
out(F) 1	C01	C03	C05	C07	C09	C11	C13	C15		C49	C51	C53	C55	C57	C59	C61	C63
out(F) 2	C01m	C03m	C05m	C07m	C09m	C11m	C13m	C15m		C49m	C51m	C53m	C55m	C57m	C59m	C61m	C63m
out(F) 3	C02	C04	C06	C08	C10	C12	C14	C16		C50	C52	C54	C56	C58	C60	C62	C64
out(F) 4	C02m	C04m	C06m	C08m	C10m	C12m	C14m	C16m		C50m	C52m	C54m	C56m	C58m	C60m	C62m	C64m

Figure D.2: TileCal patch panel crate C14 inputs and outputs

Slot	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Quadrant 2 (back panel)									Quadrant 3 (back panel)							
in(R) 1	EBA17	EBA19	EBA21	EBA23	EBA25	EBA27	EBA29	EBA31		EBA33	EBA35	EBA37	EBA39	EBA41	EBA43	EBA45	EBA47
in(R) 2	LBA17	LBA19	LBA21	LBA23	LBA25	LBA27	LBA29	LBA31		LBA33	LBA35	LBA37	LBA39	LBA41	LBA43	LBA45	LBA47
in(R) 3	EBA18	EBA20	EBA22	EBA24	EBA26	EBA28	EBA30	EBA32		EBA34	EBA36	EBA38	EBA40	EBA42	EBA44	EBA46	EBA48
in(R) 4	LBA18	LBA20	LBA22	LBA24	LBA26	LBA28	LBA30	LBA32		LBA34	LBA36	LBA38	LBA40	LBA42	LBA44	LBA46	LBA48
	Quadrant 2 (front panel)									Quadrant 3 (front panel)							
out(F) 1	A17	A19	A21	A23	A25	A27	A29	A31		A33	A35	A37	A39	A41	A43	A45	A47
out(F) 2	A17m	A19m	A21m	A23m	A25m	A27m	A29m	A31m		A33m	A35m	A37m	A39m	A41m	A43m	A45m	A47m
out(F) 3	A18	A20	A22	A24	A26	A28	A30	A32		A34	A36	A38	A40	A42	A44	A46	A48
out(F) 4	A18m	A20m	A22m	A24m	A26m	A28m	A30m	A32m		A34m	A36m	A38m	A40m	A42m	A44m	A46m	A48m

Figure D.3: TileCal patch panel crate A23 inputs and outputs

Slot	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Quadrant 1 (back panel)									Quadrant 4 (back panel)							
in(R) 1	EBA01	EBA03	EBA05	EBA07	EBA09	EBA11	EBA13	EBA15		EBA49	EBA51	EBA53	EBA55	EBA57	EBA59	EBA61	EBA63
in(R) 2	LBA01	LBA03	LBA05	LBA07	LBA09	LBA11	LBA13	LBA15		LBA49	LBA51	LBA53	LBA55	LBA57	LBA59	LBA61	LBA63
in(R) 3	EBA02	EBA04	EBA06	EBA08	EBA10	EBA12	EBA14	EBA16		EBA50	EBA52	EBA54	EBA56	EBA58	EBA60	EBA62	EBA64
in(R) 4	LBA02	LBA04	LBA06	LBA08	LBA10	LBA12	LBA14	LBA16		LBA50	LBA52	LBA54	LBA56	LBA58	LBA60	LBA62	LBA64
	Quadrant 1 (front panel)									Quadrant 4 (front panel)							
out(F) 1	A01	A03	A05	A07	A09	A11	A13	A15		A49	A51	A53	A55	A57	A59	A61	A63
out(F) 2	A01m	A03m	A05m	A07m	A09m	A11m	A13m	A15m		A49m	A51m	A53m	A55m	A57m	A59m	A61m	A63m
out(F) 3	A02	A04	A06	A08	A10	A12	A14	A16		A50	A52	A54	A56	A58	A60	A62	A64
out(F) 4	A02m	A04m	A06m	A08m	A10m	A12m	A14m	A16m		A50m	A52m	A54m	A56m	A58m	A60m	A62m	A64m

Figure D.4: TileCal patch panel crate A14 inputs and outputs

Receiver to PPM Patch Panel Crate C0 (rack Y.23-02.A2 top): PPM4-had

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	Slot
	PPM4-had Q1					PPM4-had Q2						PPM4-had Q3					PPM4-had Q4					
top	HE4b	HE4		HF4	HF4b	HA4b	HA4		HB4	HB4b		H64b	H64		H74	H74b	H24b	H24		H34	H34b	top
bottom	HC4b	HC4	HC4e	HD4	HD4b	H84b	H84	H84e	H94	H94b		H44b	H44	H44e	H54	H54b	H04b	H04	H04e	H14	H14b	bottom
Type	4	4	4	4	4	4	4	4	4	4		4	4	4	4	4	4	4	4	4	4	Type

Receiver to PPM Patch Panel Crate C1 (rack Y.23-02.A2 middle): PPM4-em

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	Slot
		PPM4-em Q1					PPM4-em Q2					PPM4-em Q3					PPM4-em Q4					
in1		EF4e	EE4e	ED4e	EC4e		EB4e	EA4e	E94e	E84e		E74e	E64e	E54e	E44e		E34e	E24e	E14e	E04e		in1
in2		EF4b	EE4b	ED4b	EC4b		EB4b	EA4b	E94b	E84b		E74b	E64b	E54b	E44b		E34b	E24b	E14b	E04b		in2
outA		EF4	EE4	ED4	EC4		EB4	EA4	E94	E84		E74	E64	E54	E44		E34	E24	E14	E04		outA
Type		1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1		Type

Receiver to PPM Patch Panel Crate C2 (rack Y.23-02.A2 bottom): PPM7 and PPM9

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	Slot
	PPM7-em Q1-4								PPM7-had Q1-4									PPM9-had (FCAL)				
in1	E01o	E21o	E41o	E61o	E81o	EA1o	EC1o	EE1o	H01o	H21o	H41o	H61o	H81o	HA1o	HC1o	HE1o		H0Zx	H4Zx	H8Zx	HCZx	in1
outA	E01	E21	E41	E61	E81	EA1	EC1	EE1	H01	H21	H41	H61	H81	HA1	HC1	HE1		H0Zy	H4Zy	H8Zy	HCZy	in2
outB	E11	E31	E51	E71	E91	EB1	ED1	EF1	H11	H31	H51	H71	H91	HB1	HD1	HF1		H0Z	H4Z	H8Z	HCZ	outA
Type	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2		6	6	6	6	Type

Figure D.5: Receiver to PPM patch panel rack C inputs and outputs

Receiver to PPM Patch Panel Crate A0 (rack Y.9-02.A2 top): PPM4-had

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	Slot
	PPM4-had Q1					PPM4-had Q2						PPM4-had Q3					PPM4-had Q4					
top	HEBb	HEB		HFB	HFBb	HABb	HAB		HBB	HBBb		H6Bb	H6B		H7B	H7Bb	H2Bb	H2B		H3B	H3Bb	top
bottom	HCBb	HCB	HCBe	HDB	HDBb	H8Bb	H8B	H8Be	H9B	H9Bb		H4Bb	H4B	H4Be	H5B	H5Bb	H0Bb	H0B	H0Be	H1B	H1Bb	bottom
Type	5	5	5	5	5	5	5	5	5	5		5	5	5	5	5	5	5	5	5	5	Type

Receiver to PPM Patch Panel Crate A1 (rack Y.9-02.A2 middle): PPM4-em

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	Slot
		PPM4-em Q1					PPM4-em Q2					PPM4-em Q3					PPM4-em Q4					
in1		EFBb	EEBb	EDBb	ECBb		EBBb	EABb	E9Bb	E8Bb		E7Bb	E6Bb	E5Bb	E4Bb		E3Bb	E2Bb	E1Bb	E0Bb		in1
in2		EFBe	EEBe	EDBe	ECBe		EBBe	EABe	E9Be	E8Be		E7Be	E6Be	E5Be	E4Be		E3Be	E2Be	E1Be	E0Be		in2
outA		EFB	EEB	EDB	ECB		EBB	EAB	E9B	E8B		E7B	E6B	E5B	E4B		E3B	E2B	E1B	E0B		outA
Type		1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1		Type

Receiver to PPM Patch Panel Crate A2 (rack Y.9-02.A2 bottom): PPM7 and PPM9

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	Slot
	PPM7-em Q1-4								PPM7-had Q1-4									PPM9-had (FCAL)				
in1	E0Eo	E2Eo	E4Eo	E6Eo	E8Eo	EAEo	ECEo	EEEo	H0Eo	H2Eo	H4Eo	H6Eo	H8Eo	HAEo	HCEo	HEEo		H0Gx	H4Gx	H8Gx	HCGx	in1
outA	E0E	E2E	E4E	E6E	E8E	EAE	ECE	EEE	H0E	H2E	H4E	H6E	H8E	HAE	HCE	HEE		H0Gy	H4Gy	H8Gy	HCGy	in2
outB	E1E	E3E	E5E	E7E	E9E	EBE	EDE	EFE	H1E	H3E	H5E	H7E	H9E	HBE	HDE	HFE		H0G	H4G	H8G	HCG	outA
Type	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3		6	6	6	6	Type

Figure D.6: Receiver to PPM patch panel rack A inputs and outputs

E Preprocessor crate module and cabling details

This appendix details all of the analogue input cables and LVDS output cables of the 124 Preprocessor modules in the system, and how these modules are divided into crates. There are eight figures corresponding to each of the eight crates. These figures are composed of tables with the horizontal axis corresponding to the PPM modules as seen from the front of the crate. The vertical axis specifies the input/output cable slots, and the contents show the name of the cable connected in each slot. The vertical axis corresponds to the physical ordering of connectors, with increasing phi running downwards on both the cables and the module. Note that the input cables (in 1–4) in the tables, are on the front panel, whereas all of the LVDS outputs come from the back of the PPMs. Quadrant numbers for each module are also indicated for information.

Shading is used to highlight some of the features of the tables, though it is not necessary to be able to see these to understand the cable specifications. Most of the shading is used for the LVDS output cables. The 'standard' core region cables are unshaded, but special cables, and cables which consist of duplicated outputs which form the fanout to adjacent quadrants in phi, are shaded in different colours. A key is given in figure E.

Quadrant Number
Standard region, same quadrant
Standard region, next quadrant(s)
Extreme endcap (PPM8) region
FCAL (PPM9) region

Figure E: Colouring key for PPM crate tables.

Preprocessor crate 0: EM Barrel +Z (A side)

Slot	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Conn	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
in 1	E08	E09	E0A	E0B	E48	E49	E4A	E4B	E88	E89	E8A	E8B	EC8	EC9	ECA	ECB
in 2	E18	E19	E1A	E1B	E58	E59	E5A	E5B	E98	E99	E9A	E9B	ED8	ED9	EDA	EDB
in 3	E28	E29	E2A	E2B	E68	E69	E6A	E6B	EA8	EA9	EAA	EAB	EE8	EE9	EEA	EEB
in 4	E38	E39	E3A	E3B	E78	E79	E7A	E7B	EB8	EB9	EBA	EBB	EF8	EF9	EFA	EFB
W	E18w	E19w	E1Aw	E1Bw	E28w	E29w	E2Aw	E2Bw	E38w	E39w	E3Aw	E3Bw	E48w	E49w	E4Aw	E4Bw
A	E18a	E19a	E1Aa	E1Ba	E28a	E29a	E2Aa	E2Ba	E38a	E39a	E3Aa	E3Ba	E48a	E49a	E4Aa	E4Ba
B	E18b	E19b	E1Ab	E1Bb	E28b	E29b	E2Ab	E2Bb	E38b	E39b	E3Ab	E3Bb	E48b	E49b	E4Ab	E4Bb
C	E18c	E19c	E1Ac	E1Bc	E28c	E29c	E2Ac	E2Bc	E38c	E39c	E3Ac	E3Bc	E48c	E49c	E4Ac	E4Bc
D	E18d	E19d	E1Ad	E1Bd	E28d	E29d	E2Ad	E2Bd	E38d	E39d	E3Ad	E3Bd	E48d	E49d	E4Ad	E4Bd
E	E18e	E19e	E1Ae	E1Be	E28e	E29e	E2Ae	E2Be	E38e	E39e	E3Ae	E3Be	E48e	E49e	E4Ae	E4Be
F	E18f	E19f	E1Af	E1Bf	E28f	E29f	E2Af	E2Bf	E38f	E39f	E3Af	E3Bf	E48f	E49f	E4Af	E4Bf
G	E18g	E19g	E1Ag	E1Bg	E28g	E29g	E2Ag	E2Bg	E38g	E39g	E3Ag	E3Bg	E48g	E49g	E4Ag	E4Bg
H	E18h	E19h	E1Ah	E1Bh	E28h	E29h	E2Ah	E2Bh	E38h	E39h	E3Ah	E3Bh	E48h	E49h	E4Ah	E4Bh
V	E18v	E19v	E1Av	E1Bv	E28v	E29v	E2Av	E2Bv	E38v	E39v	E3Av	E3Bv	E48v	E49v	E4Av	E4Bv
F1																
F2																
V8																
WX	E18wx	E19wx	E1Awx	E1Bwx	E28wx	E29wx	E2Awx	E2Bwx	E38wx	E39wx	E3Awx	E3Bwx	E48wx	E49wx	E4Awx	E4Bwx
AB	E18ab	E19ab	E1Aab	E1Bab	E28ab	E29ab	E2Aab	E2Bab	E38ab	E39ab	E3Aab	E3Bab	E48ab	E49ab	E4Aab	E4Bab
CD	E18cd	E19cd	E1Acd	E1Bcd	E28cd	E29cd	E2Acd	E2Bcd	E38cd	E39cd	E3Acd	E3Bcd	E48cd	E49cd	E4Acd	E4Bcd
EF	E18ef	E19ef	E1Aef	E1Bef	E28ef	E29ef	E2Aef	E2Bef	E38ef	E39ef	E3Aef	E3Bef	E48ef	E49ef	E4Aef	E4Bef
GH	E18gh	E19gh	E1Agh	E1Bgh	E28gh	E29gh	E2Agh	E2Bgh	E38gh	E39gh	E3Agh	E3Bgh	E48gh	E49gh	E4Agh	E4Bgh
VJ	E18vj	E19vj	E1Avj	E1Bvj	E28vj	E29vj	E2Avj	E2Bvj	E38vj	E39vj	E3Avj	E3Bvj	E48vj	E49vj	E4Avj	E4Bvj
W8																
F3																
F4																

Figure E.1: Preprocessor crate 0 inputs and outputs

Preprocessor crate 1: EM Barrel -Z (C side)

Slot	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Conn	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
in 1	E04	E05	E06	E07	E44	E45	E46	E47	E84	E85	E86	E87	EC4	EC5	EC6	EC7
in 2	E14	E15	E16	E17	E54	E55	E56	E57	E94	E95	E96	E97	ED4	ED5	ED6	ED7
in 3	E24	E25	E26	E27	E64	E65	E66	E67	EA4	EA5	EA6	EA7	EE4	EE5	EE6	EE7
in 4	E34	E35	E36	E37	E74	E75	E76	E77	EB4	EB5	EB6	EB7	EF4	EF5	EF6	EF7
W	E14w	E15w	E16w	E17w	E24w	E25w	E26w	E27w	E34w	E35w	E36w	E37w	E44w	E45w	E46w	E47w
A	E14a	E15a	E16a	E17a	E24a	E25a	E26a	E27a	E34a	E35a	E36a	E37a	E44a	E45a	E46a	E47a
B	E14b	E15b	E16b	E17b	E24b	E25b	E26b	E27b	E34b	E35b	E36b	E37b	E44b	E45b	E46b	E47b
C	E14c	E15c	E16c	E17c	E24c	E25c	E26c	E27c	E34c	E35c	E36c	E37c	E44c	E45c	E46c	E47c
D	E14d	E15d	E16d	E17d	E24d	E25d	E26d	E27d	E34d	E35d	E36d	E37d	E44d	E45d	E46d	E47d
E	E14e	E15e	E16e	E17e	E24e	E25e	E26e	E27e	E34e	E35e	E36e	E37e	E44e	E45e	E46e	E47e
F	E14f	E15f	E16f	E17f	E24f	E25f	E26f	E27f	E34f	E35f	E36f	E37f	E44f	E45f	E46f	E47f
G	E14g	E15g	E16g	E17g	E24g	E25g	E26g	E27g	E34g	E35g	E36g	E37g	E44g	E45g	E46g	E47g
H	E14h	E15h	E16h	E17h	E24h	E25h	E26h	E27h	E34h	E35h	E36h	E37h	E44h	E45h	E46h	E47h
V	E14v	E15v	E16v	E17v	E24v	E25v	E26v	E27v	E34v	E35v	E36v	E37v	E44v	E45v	E46v	E47v
F1																
F2																
V8																
WX	E14wx	E15wx	E16wx	E17wx	E24wx	E25wx	E26wx	E27wx	E34wx	E35wx	E36wx	E37wx	E44wx	E45wx	E46wx	E47wx
AB	E14ab	E15ab	E16ab	E17ab	E24ab	E25ab	E26ab	E27ab	E34ab	E35ab	E36ab	E37ab	E44ab	E45ab	E46ab	E47ab
CD	E14cd	E15cd	E16cd	E17cd	E24cd	E25cd	E26cd	E27cd	E34cd	E35cd	E36cd	E37cd	E44cd	E45cd	E46cd	E47cd
EF	E14ef	E15ef	E16ef	E17ef	E24ef	E25ef	E26ef	E27ef	E34ef	E35ef	E36ef	E37ef	E44ef	E45ef	E46ef	E47ef
GH	E14gh	E15gh	E16gh	E17gh	E24gh	E25gh	E26gh	E27gh	E34gh	E35gh	E36gh	E37gh	E44gh	E45gh	E46gh	E47gh
VJ	E14vj	E15vj	E16vj	E17vj	E24vj	E25vj	E26vj	E27vj	E34vj	E35vj	E36vj	E37vj	E44vj	E45vj	E46vj	E47vj
W8																
F3																
F4																

Figure E.2: Preprocessor crate 1 inputs and outputs

Preprocessor crate 2: EM Endcap +Z (A side)

Conn \ Slot	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
		Quadrant 1			Q12	Quadrant 2				Quadrant 3			Q34	Quadrant 4		
in 1		E0C	E0D	E0E	E0F	E4C	E4D	E4E		E8C	E8D	E8E	E8F	ECC	ECD	ECE
in 2		E1C	E1D	E1E	E2F	E5C	E5D	E5E		E9C	E9D	E9E	EAF	EDC	EDD	EDE
in 3		E2C	E2D	E2E	E4F	E6C	E6D	E6E		EAC	EAD	EAE	ECF	EEC	EED	EEE
in 4		E3C	E3D	E3E	E6F	E7C	E7D	E7E		EBC	EBD	EBE	EEF	EFC	EFD	EFE
W		E1Cw	E1Dw	E1Ew		E2Cw	E2Dw	E2Ew		E3Cw	E3Dw	E3Ew		E4Cw	E4Dw	E4Ew
A		E1Ca	E1Da	E1Ea		E2Ca	E2Da	E2Ea		E3Ca	E3Da	E3Ea		E4Ca	E4Da	E4Ea
B		E1Cb	E1Db	E1Eb		E2Cb	E2Db	E2Eb		E3Cb	E3Db	E3Eb		E4Cb	E4Db	E4Eb
C		E1Cc	E1Dc	E1Ec		E2Cc	E2Dc	E2Ec		E3Cc	E3Dc	E3Ec		E4Cc	E4Dc	E4Ec
D		E1Cd	E1Dd	E1Ed		E2Cd	E2Dd	E2Ed		E3Cd	E3Dd	E3Ed		E4Cd	E4Dd	E4Ed
E		E1Ce	E1De	E1Ee		E2Ce	E2De	E2Ee		E3Ce	E3De	E3Ee		E4Ce	E4De	E4Ee
F		E1Cf	E1Df	E1Ef		E2Cf	E2Df	E2Ef		E3Cf	E3Df	E3Ef		E4Cf	E4Df	E4Ef
G		E1Cg	E1Dg	E1Eg		E2Cg	E2Dg	E2Eg		E3Cg	E3Dg	E3Eg		E4Cg	E4Dg	E4Eg
H		E1Ch	E1Dh	E1Eh		E2Ch	E2Dh	E2Eh		E3Ch	E3Dh	E3Eh		E4Ch	E4Dh	E4Eh
V		E1Cv	E1Dv	E1Ev		E2Cv	E2Dv	E2Ev		E3Cv	E3Dv	E3Ev		E4Cv	E4Dv	E4Ev
F1																
F2																
V8					E1Fv8								E3Fv8			
WX		E1Cwx	E1Dwx	E1Ewx	E1Fwx	E2Cwx	E2Dwx	E2Ewx		E3Cwx	E3Dwx	E3Ewx	E3Fwx	E4Cwx	E4Dwx	E4Ewx
AB		E1Cab	E1Dab	E1Eab	E1Fad	E2Cab	E2Dab	E2Eab		E3Cab	E3Dab	E3Eab	E3Fad	E4Cab	E4Dab	E4Eab
CD		E1Ccd	E1Dcd	E1Ecd	E1Feh	E2Ccd	E2Dcd	E2Ecd		E3Ccd	E3Dcd	E3Ecd	E3Feh	E4Ccd	E4Dcd	E4Ecd
EF		E1Cef	E1Def	E1Eef	E2Fad	E2Cef	E2Def	E2Eef		E3Cef	E3Def	E3Eef	E4Fad	E4Cef	E4Def	E4Eef
GH		E1Cgh	E1Dgh	E1Egh	E2Feh	E2Cgh	E2Dgh	E2Egh		E3Cgh	E3Dgh	E3Egh	E4Feh	E4Cgh	E4Dgh	E4Egh
VJ		E1Cvj	E1Dvj	E1Evj	E2Fvj	E2Cvj	E2Dvj	E2Evj		E3Cvj	E3Dvj	E3Evj	E4Fvj	E4Cvj	E4Dvj	E4Evj
W8					E2Fw8								E4Fw8			
F3																
F4																

Figure E.3: Preprocessor crate 2 inputs and outputs

Preprocessor crate 3: EM Endcap -Z (C side)

Conn \ Slot	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
		Quadrant 1			Q12	Quadrant 2				Quadrant 3			Q34	Quadrant 4		
in 1		E01	E02	E03	E00	E41	E42	E43		E81	E82	E83	E80	EC1	EC2	EC3
in 2		E11	E12	E13	E20	E51	E52	E53		E91	E92	E93	EA0	ED1	ED2	ED3
in 3		E21	E22	E23	E40	E61	E62	E63		EA1	EA2	EA3	EC0	EE1	EE2	EE3
in 4		E31	E32	E33	E60	E71	E72	E73		EB1	EB2	EB3	EE0	EF1	EF2	EF3
W		E11w	E12w	E13w		E21w	E22w	E23w		E31w	E32w	E33w		E41w	E42w	E43w
A		E11a	E12a	E13a		E21a	E22a	E23a		E31a	E32a	E33a		E41a	E42a	E43a
B		E11b	E12b	E13b		E21b	E22b	E23b		E31b	E32b	E33b		E41b	E42b	E43b
C		E11c	E12c	E13c		E21c	E22c	E23c		E31c	E32c	E33c		E41c	E42c	E43c
D		E11d	E12d	E13d		E21d	E22d	E23d		E31d	E32d	E33d		E41d	E42d	E43d
E		E11e	E12e	E13e		E21e	E22e	E23e		E31e	E32e	E33e		E41e	E42e	E43e
F		E11f	E12f	E13f		E21f	E22f	E23f		E31f	E32f	E33f		E41f	E42f	E43f
G		E11g	E12g	E13g		E21g	E22g	E23g		E31g	E32g	E33g		E41g	E42g	E43g
H		E11h	E12h	E13h		E21h	E22h	E23h		E31h	E32h	E33h		E41h	E42h	E43h
V		E11v	E12v	E13v		E21v	E22v	E23v		E31v	E32v	E33v		E41v	E42v	E43v
F1																
F2																
V8					E10v8								E30v8			
WX		E11wx	E12wx	E13wx	E10wx	E21wx	E22wx	E23wx		E31wx	E32wx	E33wx	E30wx	E41wx	E42wx	E43wx
AB		E11ab	E12ab	E13ab	E10ad	E21ab	E22ab	E23ab		E31ab	E32ab	E33ab	E30ad	E41ab	E42ab	E43ab
CD		E11cd	E12cd	E13cd	E10eh	E21cd	E22cd	E23cd		E31cd	E32cd	E33cd	E30eh	E41cd	E42cd	E43cd
EF		E11ef	E12ef	E13ef	E20ad	E21ef	E22ef	E23ef		E31ef	E32ef	E33ef	E40ad	E41ef	E42ef	E43ef
GH		E11gh	E12gh	E13gh	E20eh	E21gh	E22gh	E23gh		E31gh	E32gh	E33gh	E40eh	E41gh	E42gh	E43gh
VJ		E11vj	E12vj	E13vj	E20vj	E21vj	E22vj	E23vj		E31vj	E32vj	E33vj	E40vj	E41vj	E42vj	E43vj
W8					E20w8								E40w8			
F3																
F4																

Figure E.4: Preprocessor crate 3 inputs and outputs

Preprocessor crate 4: Hadronic Endcap/FCAL +Z (A side)

Slot	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Conn	F/E	Quadrant 1			Q12	Quadrant 2			F/H	Quadrant 3			Q34	Quadrant 4		
in 1	E0G	H0C	H0D	H0E	H0F	H4C	H4D	H4E	H0G	H8C	H8D	H8E	H8F	HCC	HCD	HCE
in 2	E4G	H1C	H1D	H1E	H2F	H5C	H5D	H5E	H4G	H9C	H9D	H9E	HAF	HDC	HDD	HDE
in 3	E8G	H2C	H2D	H2E	H4F	H6C	H6D	H6E	H8G	HAC	HAD	HAE	HCF	HEC	HED	HEE
in 4	ECG	H3C	H3D	H3E	H6F	H7C	H7D	H7E	HCG	HBC	HBD	HBE	HEF	HFC	HFD	HFE
W		H1Cw	H1Dw	H1Ew		H2Cw	H2Dw	H2Ew		H3Cw	H3Dw	H3Ew		H4Cw	H4Dw	H4Ew
A		H1Ca	H1Da	H1Ea		H2Ca	H2Da	H2Ea		H3Ca	H3Da	H3Ea		H4Ca	H4Da	H4Ea
B		H1Cb	H1Db	H1Eb		H2Cb	H2Db	H2Eb		H3Cb	H3Db	H3Eb		H4Cb	H4Db	H4Eb
C		H1Cc	H1Dc	H1Ec		H2Cc	H2Dc	H2Ec		H3Cc	H3Dc	H3Ec		H4Cc	H4Dc	H4Ec
D		H1Cd	H1Dd	H1Ed		H2Cd	H2Dd	H2Ed		H3Cd	H3Dd	H3Ed		H4Cd	H4Dd	H4Ed
E		H1Ce	H1De	H1Ee		H2Ce	H2De	H2Ee		H3Ce	H3De	H3Ee		H4Ce	H4De	H4Ee
F		H1Cf	H1Df	H1Ef		H2Cf	H2Df	H2Ef		H3Cf	H3Df	H3Ef		H4Cf	H4Df	H4Ef
G		H1Cg	H1Dg	H1Eg		H2Cg	H2Dg	H2Eg		H3Cg	H3Dg	H3Eg		H4Cg	H4Dg	H4Eg
H		H1Ch	H1Dh	H1Eh		H2Ch	H2Dh	H2Eh		H3Ch	H3Dh	H3Eh		H4Ch	H4Dh	H4Eh
V		H1Cv	H1Dv	H1Ev		H2Cv	H2Dv	H2Ev		H3Cv	H3Dv	H3Ev		H4Cv	H4Dv	H4Ev
F1	E1Gf1								H1Gf1							
F2	E2Gf2								H2Gf2							
V8					H1Fv8								H3Fv8			
WX		H1Cwx	H1Dwx	H1Ewx	H1Fwx	H2Cwx	H2Dwx	H2Ewx		H3Cwx	H3Dwx	H3Ewx	H3Fwx	H4Cwx	H4Dwx	H4Ewx
AB	E1Gah	H1Cab	H1Dab	H1Eab	H1Fad	H2Cab	H2Dab	H2Eab	H1Gah	H3Cab	H3Dab	H3Eab	H3Fad	H4Cab	H4Dab	H4Eab
CD	E2Gah	H1Ccd	H1Dcd	H1Ecd	H1Feh	H2Ccd	H2Dcd	H2Ecd	H2Gah	H3Ccd	H3Dcd	H3Ecd	H3Feh	H4Ccd	H4Dcd	H4Ecd
EF	E3Gah	H1Cef	H1Def	H1Eef	H2Fad	H2Cef	H2Def	H2Eef	H3Gah	H3Cef	H3Def	H3Eef	H4Fad	H4Cef	H4Def	H4Eef
GH	E4Gah	H1Cgh	H1Dgh	H1Egh	H2Feh	H2Cgh	H2Dgh	H2Egh	H4Gah	H3Cgh	H3Dgh	H3Egh	H4Feh	H4Cgh	H4Dgh	H4Egh
VJ		H1Cvj	H1Dvj	H1Evj	H2Fvj	H2Cvj	H2Dvj	H2Evj		H3Cvj	H3Dvj	H3Evj	H4Fvj	H4Cvj	H4Dvj	H4Evj
W8					H2Fw8								H4Fw8			
F3	E3Gf3								H3Gf3							
F4	E4Gf4								H4Gf4							

Figure E.5: Preprocessor crate 4 inputs and outputs

Preprocessor crate 5: Hadronic Endcap/FCAL -Z (C side)

Slot	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Conn	F/E	Quadrant 1			Q12	Quadrant 2			F/H	Quadrant 3			Q34	Quadrant 4		
in 1	E0Z	H01	H02	H03	H00	H41	H42	H43	H0Z	H81	H82	H83	H80	HC1	HC2	HC3
in 2	E4Z	H11	H12	H13	H20	H51	H52	H53	H4Z	H91	H92	H93	HA0	HD1	HD2	HD3
in 3	E8Z	H21	H22	H23	H40	H61	H62	H63	H8Z	HA1	HA2	HA3	HC0	HE1	HE2	HE3
in 4	ECZ	H31	H32	H33	H60	H71	H72	H73	HCZ	HB1	HB2	HB3	HE0	HF1	HF2	HF3
W		H11w	H12w	H13w		H21w	H22w	H23w		H31w	H32w	H33w		H41w	H42w	H43w
A		H11a	H12a	H13a		H21a	H22a	H23a		H31a	H32a	H33a		H41a	H42a	H43a
B		H11b	H12b	H13b		H21b	H22b	H23b		H31b	H32b	H33b		H41b	H42b	H43b
C		H11c	H12c	H13c		H21c	H22c	H23c		H31c	H32c	H33c		H41c	H42c	H43c
D		H11d	H12d	H13d		H21d	H22d	H23d		H31d	H32d	H33d		H41d	H42d	H43d
E		H11e	H12e	H13e		H21e	H22e	H23e		H31e	H32e	H33e		H41e	H42e	H43e
F		H11f	H12f	H13f		H21f	H22f	H23f		H31f	H32f	H33f		H41f	H42f	H43f
G		H11g	H12g	H13g		H21g	H22g	H23g		H31g	H32g	H33g		H41g	H42g	H43g
H		H11h	H12h	H13h		H21h	H22h	H23h		H31h	H32h	H33h		H41h	H42h	H43h
V		H11v	H12v	H13v		H21v	H22v	H23v		H31v	H32v	H33v		H41v	H42v	H43v
F1	E1Zf1								H1Zf1							
F2	E2Zf2								H2Zf2							
V8					H10v8								H30v8			
WX		H11wx	H12wx	H13wx	H10wx	H21wx	H22wx	H23wx		H31wx	H32wx	H33wx	H30wx	H41wx	H42wx	H43wx
AB	E1Zah	H11ab	H12ab	H13ab	H10ad	H21ab	H22ab	H23ab	H1Zah	H31ab	H32ab	H33ab	H30ad	H41ab	H42ab	H43ab
CD	E2Zah	H11cd	H12cd	H13cd	H10eh	H21cd	H22cd	H23cd	H2Zah	H31cd	H32cd	H33cd	H30eh	H41cd	H42cd	H43cd
EF	E3Zah	H11ef	H12ef	H13ef	H20ad	H21ef	H22ef	H23ef	H3Zah	H31ef	H32ef	H33ef	H40ad	H41ef	H42ef	H43ef
GH	E4Zah	H11gh	H12gh	H13gh	H20eh	H21gh	H22gh	H23gh	H4Zah	H31gh	H32gh	H33gh	H40eh	H41gh	H42gh	H43gh
VJ		H11vj	H12vj	H13vj	H20vj	H21vj	H22vj	H23vj		H31vj	H32vj	H33vj	H40vj	H41vj	H42vj	H43vj
W8					H20w8								H40w8			
F3	E3Zf3								H3Zf3							
F4	E4Zf4								H4Zf4							

Figure E.6: Preprocessor crate 5 inputs and outputs

Preprocessor crate 6: Hadronic Barrel +Z (A side)

Conn	Slot 5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
in 1	H08	H09	H0A	H0B	H48	H49	H4A	H4B	H88	H89	H8A	H8B	HC8	HC9	HCA	HCB
in 2	H18	H19	H1A	H1B	H58	H59	H5A	H5B	H98	H99	H9A	H9B	HD8	HD9	HDA	HDB
in 3	H28	H29	H2A	H2B	H68	H69	H6A	H6B	HA8	HA9	HAA	HAB	HE8	HE9	HEA	HEB
in 4	H38	H39	H3A	H3B	H78	H79	H7A	H7B	HB8	HB9	HBA	HBB	HF8	HF9	HFA	HFB
W	H18w	H19w	H1Aw	H1Bw	H28w	H29w	H2Aw	H2Bw	H38w	H39w	H3Aw	H3Bw	H48w	H49w	H4Aw	H4Bw
A	H18a	H19a	H1Aa	H1Ba	H28a	H29a	H2Aa	H2Ba	H38a	H39a	H3Aa	H3Ba	H48a	H49a	H4Aa	H4Ba
B	H18b	H19b	H1Ab	H1Bb	H28b	H29b	H2Ab	H2Bb	H38b	H39b	H3Ab	H3Bb	H48b	H49b	H4Ab	H4Bb
C	H18c	H19c	H1Ac	H1Bc	H28c	H29c	H2Ac	H2Bc	H38c	H39c	H3Ac	H3Bc	H48c	H49c	H4Ac	H4Bc
D	H18d	H19d	H1Ad	H1Bd	H28d	H29d	H2Ad	H2Bd	H38d	H39d	H3Ad	H3Bd	H48d	H49d	H4Ad	H4Bd
E	H18e	H19e	H1Ae	H1Be	H28e	H29e	H2Ae	H2Be	H38e	H39e	H3Ae	H3Be	H48e	H49e	H4Ae	H4Be
F	H18f	H19f	H1Af	H1Bf	H28f	H29f	H2Af	H2Bf	H38f	H39f	H3Af	H3Bf	H48f	H49f	H4Af	H4Bf
G	H18g	H19g	H1Ag	H1Bg	H28g	H29g	H2Ag	H2Bg	H38g	H39g	H3Ag	H3Bg	H48g	H49g	H4Ag	H4Bg
H	H18h	H19h	H1Ah	H1Bh	H28h	H29h	H2Ah	H2Bh	H38h	H39h	H3Ah	H3Bh	H48h	H49h	H4Ah	H4Bh
V	H18v	H19v	H1Av	H1Bv	H28v	H29v	H2Av	H2Bv	H38v	H39v	H3Av	H3Bv	H48v	H49v	H4Av	H4Bv
F1																
F2																
V8																
WX	H18wx	H19wx	H1Awx	H1Bwx	H28wx	H29wx	H2Awx	H2Bwx	H38wx	H39wx	H3Awx	H3Bwx	H48wx	H49wx	H4Awx	H4Bwx
AB	H18ab	H19ab	H1Aab	H1Bab	H28ab	H29ab	H2Aab	H2Bab	H38ab	H39ab	H3Aab	H3Bab	H48ab	H49ab	H4Aab	H4Bab
CD	H18cd	H19cd	H1Acd	H1Bcd	H28cd	H29cd	H2Acd	H2Bcd	H38cd	H39cd	H3Acd	H3Bcd	H48cd	H49cd	H4Acd	H4Bcd
EF	H18ef	H19ef	H1Aef	H1Bef	H28ef	H29ef	H2Aef	H2Bef	H38ef	H39ef	H3Aef	H3Bef	H48ef	H49ef	H4Aef	H4Bef
GH	H18gh	H19gh	H1Agh	H1Bgh	H28gh	H29gh	H2Agh	H2Bgh	H38gh	H39gh	H3Agh	H3Bgh	H48gh	H49gh	H4Agh	H4Bgh
VJ	H18vj	H19vj	H1Avj	H1Bvj	H28vj	H29vj	H2Avj	H2Bvj	H38vj	H39vj	H3Avj	H3Bvj	H48vj	H49vj	H4Avj	H4Bvj
W8																
F3																
F4																

Figure E.7: Preprocessor crate 6 inputs and outputs

Preprocessor crate 7: Hadronic Barrel -Z (C side)

Conn	Slot 5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	Quadrant 1				Quadrant 2				Quadrant 3				Quadrant 4			
in 1	H04	H05	H06	H07	H44	H45	H46	H47	H84	H85	H86	H87	HC4	HC5	HC6	HC7
in 2	H14	H15	H16	H17	H54	H55	H56	H57	H94	H95	H96	H97	HD4	HD5	HD6	HD7
in 3	H24	H25	H26	H27	H64	H65	H66	H67	HA4	HA5	HA6	HA7	HE4	HE5	HE6	HE7
in 4	H34	H35	H36	H37	H74	H75	H76	H77	HB4	HB5	HB6	HB7	HF4	HF5	HF6	HF7
W	H14w	H15w	H16w	H17w	H24w	H25w	H26w	H27w	H34w	H35w	H36w	H37w	H44w	H45w	H46w	H47w
A	H14a	H15a	H16a	H17a	H24a	H25a	H26a	H27a	H34a	H35a	H36a	H37a	H44a	H45a	H46a	H47a
B	H14b	H15b	H16b	H17b	H24b	H25b	H26b	H27b	H34b	H35b	H36b	H37b	H44b	H45b	H46b	H47b
C	H14c	H15c	H16c	H17c	H24c	H25c	H26c	H27c	H34c	H35c	H36c	H37c	H44c	H45c	H46c	H47c
D	H14d	H15d	H16d	H17d	H24d	H25d	H26d	H27d	H34d	H35d	H36d	H37d	H44d	H45d	H46d	H47d
E	H14e	H15e	H16e	H17e	H24e	H25e	H26e	H27e	H34e	H35e	H36e	H37e	H44e	H45e	H46e	H47e
F	H14f	H15f	H16f	H17f	H24f	H25f	H26f	H27f	H34f	H35f	H36f	H37f	H44f	H45f	H46f	H47f
G	H14g	H15g	H16g	H17g	H24g	H25g	H26g	H27g	H34g	H35g	H36g	H37g	H44g	H45g	H46g	H47g
H	H14h	H15h	H16h	H17h	H24h	H25h	H26h	H27h	H34h	H35h	H36h	H37h	H44h	H45h	H46h	H47h
V	H14v	H15v	H16v	H17v	H24v	H25v	H26v	H27v	H34v	H35v	H36v	H37v	H44v	H45v	H46v	H47v
F1																
F2																
V8																
WX	H14wx	H15wx	H16wx	H17wx	H24wx	H25wx	H26wx	H27wx	H34wx	H35wx	H36wx	H37wx	H44wx	H45wx	H46wx	H47wx
AB	H14ab	H15ab	H16ab	H17ab	H24ab	H25ab	H26ab	H27ab	H34ab	H35ab	H36ab	H37ab	H44ab	H45ab	H46ab	H47ab
CD	H14cd	H15cd	H16cd	H17cd	H24cd	H25cd	H26cd	H27cd	H34cd	H35cd	H36cd	H37cd	H44cd	H45cd	H46cd	H47cd
EF	H14ef	H15ef	H16ef	H17ef	H24ef	H25ef	H26ef	H27ef	H34ef	H35ef	H36ef	H37ef	H44ef	H45ef	H46ef	H47ef
GH	H14gh	H15gh	H16gh	H17gh	H24gh	H25gh	H26gh	H27gh	H34gh	H35gh	H36gh	H37gh	H44gh	H45gh	H46gh	H47gh
VJ	H14vj	H15vj	H16vj	H17vj	H24vj	H25vj	H26vj	H27vj	H34vj	H35vj	H36vj	H37vj	H44vj	H45vj	H46vj	H47vj
W8																
F3																
F4																

Figure E.8: Preprocessor crate 7 inputs and outputs

F Processor crate module and cabling details

This appendix details all of the LVDS input cables to the cluster and jet/energy processing systems, and how the processing modules are divided into crates. There are six figures corresponding to each of the six crates. These figures are composed of tables with the horizontal axis corresponding to the CPM or JEM modules as seen from the front of the crate. The vertical axis specifies the input cable slots, and the contents show the name of the cable connected in each slot. In contrast to the Preprocessor crates, increasing phi generally runs upwards on both the cables and the module. All input cables are plugged into the back of the modules through a custom backplane.

Additional to the basic slot/cable mapping, several other pieces of useful information are found around the edges of the table. This includes the slot number of the modules in the processor crates and the eta/phi region processed in each row/column (in suitable units, often using the hexadecimal system defined for receiver to input cables). Shading is used for LVDS cables in a similar way to that used for the PPM output end of the cable. The key can be found in figure E.

Cluster Processor crate 0 (quadrant 1)

Phi	BP slot	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Eta bin		**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	
	Cable	Quadrant 1															
4	1		E21w	E22w	E23w	E24w	E25w	E26w	E27w	E28w	E29w	E2Aw	E2Bw	E2Cw	E2Dw	E2Ew	
3	2		E11h	E12h	E13h	E14h	E15h	E16h	E17h	E18h	E19h	E1Ah	E1Bh	E1Ch	E1Dh	E1Eh	
4	3		H21w	H22w	H23w	H24w	H25w	H26w	H27w	H28w	H29w	H2Aw	H2Bw	H2Cw	H2Dw	H2Ew	
3	4		H11h	H12h	H13h	H14h	H15h	H16h	H17h	H18h	H19h	H1Ah	H1Bh	H1Ch	H1Dh	H1Eh	
3	5		E11g	E12g	E13g	E14g	E15g	E16g	E17g	E18g	E19g	E1Ag	E1Bg	E1Cg	E1Dg	E1Eg	
2	6		E11f	E12f	E13f	E14f	E15f	E16f	E17f	E18f	E19f	E1Af	E1Bf	E1Cf	E1Df	E1Ef	
3	7		H11g	H12g	H13g	H14g	H15g	H16g	H17g	H18g	H19g	H1Ag	H1Bg	H1Cg	H1Dg	H1Eg	
2	8		H11f	H12f	H13f	H14f	H15f	H16f	H17f	H18f	H19f	H1Af	H1Bf	H1Cf	H1Df	H1Ef	
2	9		E11e	E12e	E13e	E14e	E15e	E16e	E17e	E18e	E19e	E1Ae	E1Be	E1Ce	E1De	E1Ee	
1	10		E11d	E12d	E13d	E14d	E15d	E16d	E17d	E18d	E19d	E1Ad	E1Bd	E1Cd	E1Dd	E1Ed	
2	11		H11e	H12e	H13e	H14e	H15e	H16e	H17e	H18e	H19e	H1Ae	H1Be	H1Ce	H1De	H1Ee	
1	12		H11d	H12d	H13d	H14d	H15d	H16d	H17d	H18d	H19d	H1Ad	H1Bd	H1Cd	H1Dd	H1Ed	
1	13		E11c	E12c	E13c	E14c	E15c	E16c	E17c	E18c	E19c	E1Ac	E1Bc	E1Cc	E1Dc	E1Ec	
0	14		E11b	E12b	E13b	E14b	E15b	E16b	E17b	E18b	E19b	E1Ab	E1Bb	E1Cb	E1Db	E1Eb	
1	15		H11c	H12c	H13c	H14c	H15c	H16c	H17c	H18c	H19c	H1Ac	H1Bc	H1Cc	H1Dc	H1Ec	
0	16		H11b	H12b	H13b	H14b	H15b	H16b	H17b	H18b	H19b	H1Ab	H1Bb	H1Cb	H1Db	H1Eb	
0	17		E11a	E12a	E13a	E14a	E15a	E16a	E17a	E18a	E19a	E1Aa	E1Ba	E1Ca	E1Da	E1Ea	
F	18		E41v	E42v	E43v	E44v	E45v	E46v	E47v	E48v	E49v	E4Av	E4Bv	E4Cv	E4Dv	E4Ev	
0	19		H11a	H12a	H13a	H14a	H15a	H16a	H17a	H18a	H19a	H1Aa	H1Ba	H1Ca	H1Da	H1Ea	
F	20		H41v	H42v	H43v	H44v	H45v	H46v	H47v	H48v	H49v	H4Av	H4Bv	H4Cv	H4Dv	H4Ev	

Figure F.1: Cluster processing crate 0, LVDS inputs

Cluster Processor crate 1 (quadrant 2)

Phi	BP slot	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Eta bin		**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	
	Cable	Quadrant 2															
8	1		E31w	E32w	E33w	E34w	E35w	E36w	E37w	E38w	E39w	E3Aw	E3Bw	E3Cw	E3Dw	E3Ew	
7	2		E21h	E22h	E23h	E24h	E25h	E26h	E27h	E28h	E29h	E2Ah	E2Bh	E2Ch	E2Dh	E2Eh	
8	3		H31w	H32w	H33w	H34w	H35w	H36w	H37w	H38w	H39w	H3Aw	H3Bw	H3Cw	H3Dw	H3Ew	
7	4		H21h	H22h	H23h	H24h	H25h	H26h	H27h	H28h	H29h	H2Ah	H2Bh	H2Ch	H2Dh	H2Eh	
7	5		E21g	E22g	E23g	E24g	E25g	E26g	E27g	E28g	E29g	E2Ag	E2Bg	E2Cg	E2Dg	E2Eg	
6	6		E21f	E22f	E23f	E24f	E25f	E26f	E27f	E28f	E29f	E2Af	E2Bf	E2Cf	E2Df	E2Ef	
7	7		H21g	H22g	H23g	H24g	H25g	H26g	H27g	H28g	H29g	H2Ag	H2Bg	H2Cg	H2Dg	H2Eg	
6	8		H21f	H22f	H23f	H24f	H25f	H26f	H27f	H28f	H29f	H2Af	H2Bf	H2Cf	H2Df	H2Ef	
6	9		E21e	E22e	E23e	E24e	E25e	E26e	E27e	E28e	E29e	E2Ae	E2Be	E2Ce	E2De	E2Ee	
5	10		E21d	E22d	E23d	E24d	E25d	E26d	E27d	E28d	E29d	E2Ad	E2Bd	E2Cd	E2Dd	E2Ed	
6	11		H21e	H22e	H23e	H24e	H25e	H26e	H27e	H28e	H29e	H2Ae	H2Be	H2Ce	H2De	H2Ee	
5	12		H21d	H22d	H23d	H24d	H25d	H26d	H27d	H28d	H29d	H2Ad	H2Bd	H2Cd	H2Dd	H2Ed	
5	13		E21c	E22c	E23c	E24c	E25c	E26c	E27c	E28c	E29c	E2Ac	E2Bc	E2Cc	E2Dc	E2Ec	
4	14		E21b	E22b	E23b	E24b	E25b	E26b	E27b	E28b	E29b	E2Ab	E2Bb	E2Cb	E2Db	E2Eb	
5	15		H21c	H22c	H23c	H24c	H25c	H26c	H27c	H28c	H29c	H2Ac	H2Bc	H2Cc	H2Dc	H2Ec	
4	16		H21b	H22b	H23b	H24b	H25b	H26b	H27b	H28b	H29b	H2Ab	H2Bb	H2Cb	H2Db	H2Eb	
4	17		E21a	E22a	E23a	E24a	E25a	E26a	E27a	E28a	E29a	E2Aa	E2Ba	E2Ca	E2Da	E2Ea	
3	18		E11v	E12v	E13v	E14v	E15v	E16v	E17v	E18v	E19v	E1Av	E1Bv	E1Cv	E1Dv	E1Ev	
4	19		H21a	H22a	H23a	H24a	H25a	H26a	H27a	H28a	H29a	H2Aa	H2Ba	H2Ca	H2Da	H2Ea	
3	20		H11v	H12v	H13v	H14v	H15v	H16v	H17v	H18v	H19v	H1Av	H1Bv	H1Cv	H1Dv	H1Ev	

Figure F.2: Cluster processing crate 1, LVDS inputs

Cluster Processor crate 2 (quadrant 3)

Phi	BP slot	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Eta bin		**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	
	Cable	Quadrant 3															
C	1		E41w	E42w	E43w	E44w	E45w	E46w	E47w	E48w	E49w	E4Aw	E4Bw	E4Cw	E4Dw	E4Ew	
B	2		E31h	E32h	E33h	E34h	E35h	E36h	E37h	E38h	E39h	E3Ah	E3Bh	E3Ch	E3Dh	E3Eh	
C	3		H41w	H42w	H43w	H44w	H45w	H46w	H47w	H48w	H49w	H4Aw	H4Bw	H4Cw	H4Dw	H4Ew	
B	4		H31h	H32h	H33h	H34h	H35h	H36h	H37h	H38h	H39h	H3Ah	H3Bh	H3Ch	H3Dh	H3Eh	
B	5		E31g	E32g	E33g	E34g	E35g	E36g	E37g	E38g	E39g	E3Ag	E3Bg	E3Cg	E3Dg	E3Eg	
A	6		E31f	E32f	E33f	E34f	E35f	E36f	E37f	E38f	E39f	E3Af	E3Bf	E3Cf	E3Df	E3Ef	
B	7		H31g	H32g	H33g	H34g	H35g	H36g	H37g	H38g	H39g	H3Ag	H3Bg	H3Cg	H3Dg	H3Eg	
A	8		H31f	H32f	H33f	H34f	H35f	H36f	H37f	H38f	H39f	H3Af	H3Bf	H3Cf	H3Df	H3Ef	
A	9		E31e	E32e	E33e	E34e	E35e	E36e	E37e	E38e	E39e	E3Ae	E3Be	E3Ce	E3De	E3Ee	
9	10		E31d	E32d	E33d	E34d	E35d	E36d	E37d	E38d	E39d	E3Ad	E3Bd	E3Cd	E3Dd	E3Ed	
A	11		H31e	H32e	H33e	H34e	H35e	H36e	H37e	H38e	H39e	H3Ae	H3Be	H3Ce	H3De	H3Ee	
9	12		H31d	H32d	H33d	H34d	H35d	H36d	H37d	H38d	H39d	H3Ad	H3Bd	H3Cd	H3Dd	H3Ed	
9	13		E31c	E32c	E33c	E34c	E35c	E36c	E37c	E38c	E39c	E3Ac	E3Bc	E3Cc	E3Dc	E3Ec	
8	14		E31b	E32b	E33b	E34b	E35b	E36b	E37b	E38b	E39b	E3Ab	E3Bb	E3Cb	E3Db	E3Eb	
9	15		H31c	H32c	H33c	H34c	H35c	H36c	H37c	H38c	H39c	H3Ac	H3Bc	H3Cc	H3Dc	H3Ec	
8	16		H31b	H32b	H33b	H34b	H35b	H36b	H37b	H38b	H39b	H3Ab	H3Bb	H3Cb	H3Db	H3Eb	
8	17		E31a	E32a	E33a	E34a	E35a	E36a	E37a	E38a	E39a	E3Aa	E3Ba	E3Ca	E3Da	E3Ea	
7	18		E21v	E22v	E23v	E24v	E25v	E26v	E27v	E28v	E29v	E2Av	E2Bv	E2Cv	E2Dv	E2Ev	
8	19		H31a	H32a	H33a	H34a	H35a	H36a	H37a	H38a	H39a	H3Aa	H3Ba	H3Ca	H3Da	H3Ea	
7	20		H21v	H22v	H23v	H24v	H25v	H26v	H27v	H28v	H29v	H2Av	H2Bv	H2Cv	H2Dv	H2Ev	

Figure F.3: Cluster processing crate 2, LVDS inputs

Cluster Processor crate 3 (quadrant 4)

Phi	BP slot	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	Eta bin		**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	
	Cable	Quadrant 4															
0	1		E11w	E12w	E13w	E14w	E15w	E16w	E17w	E18w	E19w	E1Aw	E1Bw	E1Cw	E1Dw	E1Ew	
F	2		E41h	E42h	E43h	E44h	E45h	E46h	E47h	E48h	E49h	E4Ah	E4Bh	E4Ch	E4Dh	E4Eh	
0	3		H11w	H12w	H13w	H14w	H15w	H16w	H17w	H18w	H19w	H1Aw	H1Bw	H1Cw	H1Dw	H1Ew	
F	4		H41h	H42h	H43h	H44h	H45h	H46h	H47h	H48h	H49h	H4Ah	H4Bh	H4Ch	H4Dh	H4Eh	
F	5		E41g	E42g	E43g	E44g	E45g	E46g	E47g	E48g	E49g	E4Ag	E4Bg	E4Cg	E4Dg	E4Eg	
E	6		E41f	E42f	E43f	E44f	E45f	E46f	E47f	E48f	E49f	E4Af	E4Bf	E4Cf	E4Df	E4Ef	
F	7		H41g	H42g	H43g	H44g	H45g	H46g	H47g	H48g	H49g	H4Ag	H4Bg	H4Cg	H4Dg	H4Eg	
E	8		H41f	H42f	H43f	H44f	H45f	H46f	H47f	H48f	H49f	H4Af	H4Bf	H4Cf	H4Df	H4Ef	
E	9		E41e	E42e	E43e	E44e	E45e	E46e	E47e	E48e	E49e	E4Ae	E4Be	E4Ce	E4De	E4Ee	
D	10		E41d	E42d	E43d	E44d	E45d	E46d	E47d	E48d	E49d	E4Ad	E4Bd	E4Cd	E4Dd	E4Ed	
E	11		H41e	H42e	H43e	H44e	H45e	H46e	H47e	H48e	H49e	H4Ae	H4Be	H4Ce	H4De	H4Ee	
D	12		H41d	H42d	H43d	H44d	H45d	H46d	H47d	H48d	H49d	H4Ad	H4Bd	H4Cd	H4Dd	H4Ed	
D	13		E41c	E42c	E43c	E44c	E45c	E46c	E47c	E48c	E49c	E4Ac	E4Bc	E4Cc	E4Dc	E4Ec	
C	14		E41b	E42b	E43b	E44b	E45b	E46b	E47b	E48b	E49b	E4Ab	E4Bb	E4Cb	E4Db	E4Eb	
D	15		H41c	H42c	H43c	H44c	H45c	H46c	H47c	H48c	H49c	H4Ac	H4Bc	H4Cc	H4Dc	H4Ec	
C	16		H41b	H42b	H43b	H44b	H45b	H46b	H47b	H48b	H49b	H4Ab	H4Bb	H4Cb	H4Db	H4Eb	
C	17		E41a	E42a	E43a	E44a	E45a	E46a	E47a	E48a	E49a	E4Aa	E4Ba	E4Ca	E4Da	E4Ea	
B	18		E31v	E32v	E33v	E34v	E35v	E36v	E37v	E38v	E39v	E3Av	E3Bv	E3Cv	E3Dv	E3Ev	
C	19		H41a	H42a	H43a	H44a	H45a	H46a	H47a	H48a	H49a	H4Aa	H4Ba	H4Ca	H4Da	H4Ea	
B	20		H31v	H32v	H33v	H34v	H35v	H36v	H37v	H38v	H39v	H3Av	H3Bv	H3Cv	H3Dv	H3Ev	

Figure F.4: Cluster processing crate 3, LVDS inputs

Jet/Energy Processor crate 0 (quadrants 1,3)

Phi	BP slot	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	Phi
	Eta bin	**Z,0,1**	**2,3**	**4,5**	**6,7**	**8,9**	**A,B**	**C,D**	**E,F,G**	**Z,0,1**	**2,3**	**4,5**	**6,7**	**8,9**	**A,B**	**C,D**	**E,F,G**	
	Cable	Quadrant 1								Quadrant 3								
4	1	H21wx	H23wx	H25wx	H27wx	H29wx	H2Bwx	H2Dwx	H2Fw8	H41wx	H43wx	H45wx	H47wx	H49wx	H4Bwx	H4Dwx	H4Fw8	**C**
	2	E21wx	E23wx	E25wx	E27wx	E29wx	E2Bwx	E2Dwx	E2Fw8	E41wx	E43wx	E45wx	E47wx	E49wx	E4Bwx	E4Dwx	E4Fw8	
	3	H20w8	H22wx	H24wx	H26wx	H28wx	H2Awx	H2Cwx	H2Ewx	H40w8	H42wx	H44wx	H46wx	H48wx	H4Awx	H4Cwx	H4Ewx	
	4	E20w8	E22wx	E24wx	E26wx	E28wx	E2Awx	E2Cwx	E2Ewx	E40w8	E42wx	E44wx	E46wx	E48wx	E4Awx	E4Cwx	E4Ewx	
3	5	H11gh	H13gh	H15gh	H17gh	H19gh	H1Bgh	H1Dgh	H1Feh	H31gh	H33gh	H35gh	H37gh	H39gh	H3Bgh	H3Dgh	H3Feh	**B**
	6	E11gh	E13gh	E15gh	E17gh	E19gh	E1Bgh	E1Dgh	E1Feh	E31gh	E33gh	E35gh	E37gh	E39gh	E3Bgh	E3Dgh	E3Feh	
	7	H10eh	H12gh	H14gh	H16gh	H18gh	H1Agh	H1Cgh	H1Egh	H30eh	H32gh	H34gh	H36gh	H38gh	H3Agh	H3Cgh	H3Egh	
	8	E10eh	E12gh	E14gh	E16gh	E18gh	E1Agh	E1Cgh	E1Egh	E30eh	E32gh	E34gh	E36gh	E38gh	E3Agh	E3Cgh	E3Egh	
2	9	H11ef	H13ef	H15ef	H17ef	H19ef	H1Bef	H1Def	H1Gah	H31ef	H33ef	H35ef	H37ef	H39ef	H3Bef	H3Def	H3Gah	**A**
	10	E11ef	E13ef	E15ef	E17ef	E19ef	E1Bef	E1Def	E1Gah	E31ef	E33ef	E35ef	E37ef	E39ef	E3Bef	E3Def	E3Gah	
	11	H1Zah	H12ef	H14ef	H16ef	H18ef	H1Aef	H1Cef	H1Eef	H3Zah	H32ef	H34ef	H36ef	H38ef	H3Aef	H3Cef	H3Eef	
	12	E1Zah	E12ef	E14ef	E16ef	E18ef	E1Aef	E1Cef	E1Eef	E3Zah	E32ef	E34ef	E36ef	E38ef	E3Aef	E3Cef	E3Eef	
1	13	H11cd	H13cd	H15cd	H17cd	H19cd	H1Bcd	H1Dcd	H1Fad	H31cd	H33cd	H35cd	H37cd	H39cd	H3Bcd	H3Dcd	H3Fad	**9**
	14	E11cd	E13cd	E15cd	E17cd	E19cd	E1Bcd	E1Dcd	E1Fad	E31cd	E33cd	E35cd	E37cd	E39cd	E3Bcd	E3Dcd	E3Fad	
	15	H10ad	H12cd	H14cd	H16cd	H18cd	H1Acd	H1Ccd	H1Ecd	H30ad	H32cd	H34cd	H36cd	H38cd	H3Acd	H3Ccd	H3Ecd	
	16	E10ad	E12cd	E14cd	E16cd	E18cd	E1Acd	E1Ccd	E1Ecd	E30ad	E32cd	E34cd	E36cd	E38cd	E3Acd	E3Ccd	E3Ecd	
0	17	H11ab	H13ab	H15ab	H17ab	H19ab	H1Bab	H1Dab	H1Gf1	H31ab	H33ab	H35ab	H37ab	H39ab	H3Bab	H3Dab	H3Gf3	**8**
	18	E11ab	E13ab	E15ab	E17ab	E19ab	E1Bab	E1Dab	E1Gf1	E31ab	E33ab	E35ab	E37ab	E39ab	E3Bab	E3Dab	E3Gf3	
	19	H1Zf1	H12ab	H14ab	H16ab	H18ab	H1Aab	H1Cab	H1Eab	H3Zf3	H32ab	H34ab	H36ab	H38ab	H3Aab	H3Cab	H3Eab	
	20	E1Zf1	E12ab	E14ab	E16ab	E18ab	E1Aab	E1Cab	E1Eab	E3Zf3	E32ab	E34ab	E36ab	E38ab	E3Aab	E3Cab	E3Eab	
F	21	H41vj	H43vj	H45vj	H47vj	H49vj	H4Bvj	H4Dvj	H4Fvj	H21vj	H23vj	H25vj	H27vj	H29vj	H2Bvj	H2Dvj	H2Fvj	**7**
	22	E41vj	E43vj	E45vj	E47vj	E49vj	E4Bvj	E4Dvj	E4Fvj	E21vj	E23vj	E25vj	E27vj	E29vj	E2Bvj	E2Dvj	E2Fvj	
	23	H40vj	H42vj	H44vj	H46vj	H48vj	H4Avj	H4Cvj	H4Evj	H20vj	H22vj	H24vj	H26vj	H28vj	H2Avj	H2Cvj	H2Evj	
	24	E40vj	E42vj	E44vj	E46vj	E48vj	E4Avj	E4Cvj	E4Evj	E20vj	E22vj	E24vj	E26vj	E28vj	E2Avj	E2Cvj	E2Evj	

Figure F.5: Jet/energy processing crate 0, LVDS inputs

Jet/Energy Processor crate 1 (quadrants 2,4)

Phi	BP slot	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	Phi
	Eta bin	**Z,0,1**	**2,3**	**4,5**	**6,7**	**8,9**	**A,B**	**C,D**	**E,F,G**	**Z,0,1**	**2,3**	**4,5**	**6,7**	**8,9**	**A,B**	**C,D**	**E,F,G**	
	Cable	Quadrant 2								Quadrant 4								
8	1	H31wx	H33wx	H35wx	H37wx	H39wx	H3Bwx	H3Dwx	H3Fwx	H11wx	H13wx	H15wx	H17wx	H19wx	H1Bwx	H1Dwx	H1Fwx	**0**
	2	E31wx	E33wx	E35wx	E37wx	E39wx	E3Bwx	E3Dwx	E3Fwx	E11wx	E13wx	E15wx	E17wx	E19wx	E1Bwx	E1Dwx	E1Fwx	
	3	H30wx	H32wx	H34wx	H36wx	H38wx	H3Awx	H3Cwx	H3Ewx	H10wx	H12wx	H14wx	H16wx	H18wx	H1Awx	H1Cwx	H1Ewx	
	4	E30wx	E32wx	E34wx	E36wx	E38wx	E3Awx	E3Cwx	E3Ewx	E10wx	E12wx	E14wx	E16wx	E18wx	E1Awx	E1Cwx	E1Ewx	
7	5	H21gh	H23gh	H25gh	H27gh	H29gh	H2Bgh	H2Dgh	H2Feh	H41gh	H43gh	H45gh	H47gh	H49gh	H4Bgh	H4Dgh	H4Feh	**F**
	6	E21gh	E23gh	E25gh	E27gh	E29gh	E2Bgh	E2Dgh	E2Feh	E41gh	E43gh	E45gh	E47gh	E49gh	E4Bgh	E4Dgh	E4Feh	
	7	H20eh	H22gh	H24gh	H26gh	H28gh	H2Agh	H2Cgh	H2Egh	H40eh	H42gh	H44gh	H46gh	H48gh	H4Agh	H4Cgh	H4Egh	
	8	E20eh	E22gh	E24gh	E26gh	E28gh	E2Agh	E2Cgh	E2Egh	E40eh	E42gh	E44gh	E46gh	E48gh	E4Agh	E4Cgh	E4Egh	
6	9	H21ef	H23ef	H25ef	H27ef	H29ef	H2Bef	H2Def	H2Gah	H41ef	H43ef	H45ef	H47ef	H49ef	H4Bef	H4Def	H4Gah	**E**
	10	E21ef	E23ef	E25ef	E27ef	E29ef	E2Bef	E2Def	E2Gah	E41ef	E43ef	E45ef	E47ef	E49ef	E4Bef	E4Def	E4Gah	
	11	H2Zah	H22ef	H24ef	H26ef	H28ef	H2Aef	H2Cef	H2Eef	H4Zah	H42ef	H44ef	H46ef	H48ef	H4Aef	H4Cef	H4Eef	
	12	E2Zah	E22ef	E24ef	E26ef	E28ef	E2Aef	E2Cef	E2Eef	E4Zah	E42ef	E44ef	E46ef	E48ef	E4Aef	E4Cef	E4Eef	
5	13	H21cd	H23cd	H25cd	H27cd	H29cd	H2Bcd	H2Dcd	H2Fad	H41cd	H43cd	H45cd	H47cd	H49cd	H4Bcd	H4Dcd	H4Fad	**D**
	14	E21cd	E23cd	E25cd	E27cd	E29cd	E2Bcd	E2Dcd	E2Fad	E41cd	E43cd	E45cd	E47cd	E49cd	E4Bcd	E4Dcd	E4Fad	
	15	H20ad	H22cd	H24cd	H26cd	H28cd	H2Acd	H2Ccd	H2Ecd	H40ad	H42cd	H44cd	H46cd	H48cd	H4Acd	H4Ccd	H4Ecd	
	16	E20ad	E22cd	E24cd	E26cd	E28cd	E2Acd	E2Ccd	E2Ecd	E40ad	E42cd	E44cd	E46cd	E48cd	E4Acd	E4Ccd	E4Ecd	
4	17	H21ab	H23ab	H25ab	H27ab	H29ab	H2Bab	H2Dab	H2Gf2	H41ab	H43ab	H45ab	H47ab	H49ab	H4Bab	H4Dab	H4Gf4	**C**
	18	E21ab	E23ab	E25ab	E27ab	E29ab	E2Bab	E2Dab	E2Gf2	E41ab	E43ab	E45ab	E47ab	E49ab	E4Bab	E4Dab	E4Gf4	
	19	H2Zf2	H22ab	H24ab	H26ab	H28ab	H2Aab	H2Cab	H2Eab	H4Zf4	H42ab	H44ab	H46ab	H48ab	H4Aab	H4Cab	H4Eab	
	20	E2Zf2	E22ab	E24ab	E26ab	E28ab	E2Aab	E2Cab	E2Eab	E4Zf4	E42ab	E44ab	E46ab	E48ab	E4Aab	E4Cab	E4Eab	
3	21	H11vj	H13vj	H15vj	H17vj	H19vj	H1Bvj	H1Dvj	H1Fv8	H31vj	H33vj	H35vj	H37vj	H39vj	H3Bvj	H3Dvj	H3Fv8	**B**
	22	E11vj	E13vj	E15vj	E17vj	E19vj	E1Bvj	E1Dvj	E1Fv8	E31vj	E33vj	E35vj	E37vj	E39vj	E3Bvj	E3Dvj	E3Fv8	
	23	H10v8	H12vj	H14vj	H16vj	H18vj	H1Avj	H1Cvj	H1Evj	H30v8	H32vj	H34vj	H36vj	H38vj	H3Avj	H3Cvj	H3Evj	
	24	E10v8	E12vj	E14vj	E16vj	E18vj	E1Avj	E1Cvj	E1Evj	E30v8	E32vj	E34vj	E36vj	E38vj	E3Avj	E3Cvj	E3Evj	

Figure F.6: Jet/energy processing crate 1, LVDS inputs

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